Regrowth Applied to N-type Modulation-doped Si/SiGe Heterostructures

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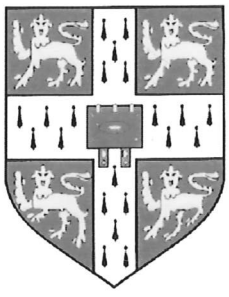

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Thesis Title:

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Conventional silicon/silicon-germanium (Si/SiGe) two dimensional electron gas (2DEG) heterostructures formed by modulation-doping, require a SiGe virtual substrate grown on a Si substrate. Active heterolayers are grown on this virtual substrate, usually in a single step process.

This dissertation describes the growth of Si/SiGe wafers in a two stage process. The virtual substrate is removed from growth system and is cleaned *ex-situ*. The wafer is then returned to the growth chamber for the deposition of the active heterolayers, introducing a regrowth interface. The successful incorporation of this regrowth interface is shown along with an investigation into the effects of the interface on transport properties.

A temperature gradient across the substrate heater, in the growth system that has been used, leads to a variation in the wafer structure. One useful consequence of this thermal gradient is that it is possible to use a single wafer to study the effect on the transport properties as a function of the Ge fraction, dopant concentration, quantum well depth and width.

The introduction of arsine as an n-type dopant into the growth chamber results in all subsequent material being n-type due to surface segregation. An *ex-situ* ion implantation technique has been developed which can be used to form a modulation-doped region in an inverted Si/SiGe 2DEG. Forming a doped region *ex-situ* circumvents the need to introduce a dopant species into the growth system, preventing surface segregation. Low temperature measurements of devices fabricated using this technique are presented, showing that it is possible to form inverted Si/SiGe 2DEGs and that *ex-situ* ion implantation can be used to form dopant supply regions.

This technique is subsequently developed to show selective area *ex-situ* ion implantation technique. The successful production of samples shows that selective doping in exact areas of a wafer during growth is feasible and this has important consequences in device production.

To My Parents

Acknowledgments

This dissertation is the result of research carried out in the Semiconductor Physics Group at the Cavendish Laboratory between October 1996 and September 2000. In the course of my research here at the Cavendish Laboratory, I have benefited greatly from the help and expertise of a large number of people. First, I must thank Professor Mike Pepper, who has both acted as my supervisor during that time and given me the opportunity to work in this group.

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I wish to acknowledge the financial support I have received during the course of this work, which has come from the EPSRC, the Cavendish Laboratory and DERA Case Award.

DECLARATION

This dissertation contains my own original work and includes nothing that is the result of work done in collaboration, except where specifically acknowledged. This dissertation is not the same as any other that I have submitted or am submitting for a degree, diploma or any other qualification at this or any other University.

This dissertation is less than 60,000 words in length.

Ataf Ahmed

September 2000

PREFACE

Conventional high performance silicon/silicon-germanium two dimensional electron gas (2DEG)heterostructures formed by modulation-doping require a SiGe virtual substrate grown on a Si substrate, since high quality SiGe substrates are not available. The active heterolayers are grown on this virtual substrate and in most growth systems the entire wafer is grown in a single step.

This dissertation describes the growth of Si/SiGe wafer in a two stage process. After the initial growth of the virtual substrate, the wafer is removed from an ultra-high vacuum (UHV) compatible chemical vapour deposition (CVD) growth chamber and is cleaned *ex-situ*. The wafer is then returned to the UHV compatible CVD chamber for the growth of the active heterolayers. This two stage process introduces a regrowth interface that affects subsequent electronic properties of fabricated devices. The successful incorporation of a regrowth interface is shown here along with an investigation into the effects of this interface on the transport properties. The regrowth process demonstrates that it is possible to treat a virtual substrate as a normal Si substrate.

A temperature gradient across the substrate heater, in the UHV compatible CVD growth chamber used to grow most wafers used during the course of this thesis, leads to a variation in the wafer structure. While the thermal gradient prevents the use of the system for manufacture, it allows the investigation of electronic properties as a function of growth parameters with the growth of only a few wafers and using only one wafer it is possible to study the effect on the transport properties as a function of the Ge fraction, dopant concentration as well as the quantum well depth and width. Since the samples are from the same wafer they will have the same background impurity concentration and will have been subjected to the same growth conditions.

The introduction of arsine (AsH_3) as a n-type dopant into the growth chamber results in all subsequent material being n-type due to surface segregation. A technique has been developed that involves the use of *ex-situ* ion implantation in forming a modulation-doped region in an inverted Si/SiGe 2DEG. By forming a doped region *ex-situ*, it circumvents the need to introduce a dopant species

into the growth system which prevents surface segregation. Low temperature measurements of devices fabricated using this technique are presented, which show that it is possible to form inverted Si/SiGe 2DEGs and that *ex-situ* ion implantation can be used to form a dopant supply region.

This technique is subsequently developed to show selective area *ex-situ* ion implantation technique.This has been used to define dopant regions in exact areas in a wafer during growth and this simplifies post-wafer growth sample processing. The successful production of samples show that selective doping is feasible and this has important consequences in device production.

Results from this research have been published or are to be published in the following articles:

D. J. Paul, A. Ahmed, N. Griffin, M. Pepper, A. C. Churchill, D. J. Robbins and D. J. Wallis, '*Electrical properties of two dimensional electron gases grown on cleaned SiGe virtual substrates*', Thin Solid Films **321**, 181 (1998).

D.J. Paul, A. Ahmed, M. Pepper, A. C. Churchill, D. J. Robbins and D.J. Wallis, '*Electrical properties of two dimensional electron gases grown on cleaned SiGe virtual substrates*', Journal of Vacuum Science and Technology B **16(3)**, 1644 (1998).

A. Ahmed, R. B. Dunford, D. J. Paul, M. Pepper, A. C. Churchill, D. J. Robbins and A. J. Pidduck, '*Si/SiGe n-type Inverted Modulation-Doping Using Ion Implantation*', Thin Solid Films **369**, 324 (2000).

R. B. Dunford, A. Ahmed, D. J. Paul, M. Pepper, A. C. Churchill, D. J. Robbins and A. J. Pidduck, '*Inverted Modulation-Doping n-typeSi/SiGe Heterostructures*', Microelectronic Engineering **53**, 205 (2000).

A. Ahmed, D. J. Paul, P. See, N. J. Curson, A. C. Churchill, W. Y. Leong, D. J. Robbins, D. J. Wallis, J. M. Newey and A. J. Pidduck, '*Uniformity of Modulation-doped Two-Dimensional Electron Gases Grown on Cleaned $Si_{1-x}Ge_x$ Virtual Substrates*', Semiconductor Science Technology (to be published).

Contents

Chapter 1

Silicon/Silicon-Germanium Material System

1.1 Thesis Structure

The structure of this thesis is as follows. This chapter reviews the silicon/silicon-germanium (SiGe[1]) material system. Particular emphasis is placed on strained layer growth, band structure and the effects of strain. The following chapter discusses some basic concepts on the transport of charged carrier in two dimensional gases in different regimes such as in electric or magnetic fields.

Chapter three contains a brief review of the growth systems that were used to provide wafers during the course of this thesis. There is also a summary of the techniques used in the fabrication of devices for electrical assessment. There is also an outline of some of the non-electrical assessment techniques that were used to provide details of wafer structure and surface morphology.

The subsequent four chapters detail experimental results that were obtained in this thesis. Chapter four presents the results from typical two dimensional electron gas (2DEG) samples and two dimensional hole gas (2DHG) samples that were used in this thesis. This chapter describes a regrowth technique that utilises an *ex-situ* chemical clean. This shows the possibility of treating a silicon-germanium virtual substrate as normal substrate. The successful incorporation of the regrowth interface in working devices is shown along with an investigation into the effects of this interface on the transport properties.

[1]Unless stated otherwise, throughout this thesis SiGe and AlGaAS refer to alloys of $Si_{1-x}Ge_x$ and $Al_xGa_{1-x}As$, with the arbitrary composition, x, being implicit

The ultra-high vacuum, chemical vapour deposition growth chamber that has been used to grow most of the wafers used in this thesis, has a temperature gradient across the substrate heater. Chapter five explores the change in uniformity in structure and electronic properties caused by the temperature gradient.

Chapter six describes a technique that combines *ex-situ* ion implantation of dopant with the regrowth technique that has been developed. This combined growth technique allows the *ex-situ* doping of wafers and it is shown in this chapter how it may be used to produce working inverted silicon/silicon-germanium 2DEG samples.

A selective area *ex-situ* doping technique that has been developed is presented in chapter seven. The combined *ex-situ* dopant implantation and regrowth technique presented in chapter six has been further developed. A modified wafer growth and device fabrication process is described that allows precision doping and results are presented from devices that have been fabricated using this technique. It is shown that selective area dopant patterning is possible and can be used to define dopant regions in a wafer during growth.

Finally chapter eight presents a summary of the conclusions and a discussion of some further investigations which lead on from the work presented in this thesis.

1.2 Introduction to Si Technologies

Since the fabrication of the first solid-state transistor in 1947 [1], semiconductor devices and materials have revolutionised consumer electronics and have changed our everyday lives.

The most extensively used material over the last fifty years has been Si. It continues to dominate global semiconductor markets, accounting for more than 98% of sales [2], with billions of dollars invested in Si based technology. This dominance can be attributed to the versatility of Si, its low cost as well as a mature wide scale manufacturing technology.

Si has high mechanical strength and a large thermal conductivity making it ideal for integration within densely packed integrated circuits, where a lot of heat can be easily generated and dissipated. The naturally occurring oxide in Si is an excellent insulator utilised extensively in device fabrication. Techniques used to purify and grow Si were first developed in the 1950s and it is now possible to

produce Si wafers with unmatched purity and perfection, cheaply and easily.

In the past few decades, the main improvements in the speed and versatility of Si electronics have mostly resulted from the miniaturization of circuitry. In the 1960s it was found that SiO_2 was able to passivate Si surface states [3] allowing electric fields from a gate oxide on the surface to penetrate into the Si and modulate electron or hole transport in a transistor. Consequently, in the 1960's the world's first field effect transistors (FETs) were produced [4]. Metal-oxide-semiconductor field effect transistors (MOSFETs) and MOS technology proved to be a cheap method of gaining higher device packing densities than non solid-state based technology with its low power consumption.

In the late 1960s Gordon Moore predicted an exponential growth of microprocessor complexity and that for fixed areas the number of transistors would double every 18 months. There would be an associated increase in the speed and performance of computers, as well as a reduction in the price. So far 'Moore's Law' has given an accurate prediction of the trends within the semiconductor industry. Si based technology, however will not be able to indefinitely cope with the demand for exponential increases in performance [5].

The main strategy adopted by the semiconductor industry for improving the operation of Si based devices is by scaling. Scaling involves enhancing the performance of a single device by reducing its size. As scaling becomes ever more expensive and as device sizes become increasingly smaller (sub-0.1 μm), fundamental quantum mechanical limits on performance are encountered. Integrated circuit designers are beginning to push scaling to its limits and it is feared that traditional technology cannot attain higher speeds without devices being shrunk to the point where they cannot function [6].

One consequence of the heavy investment in Si based technologies is that many companies are reluctant to re-invest the large amount of capital that would be required to shift to an alternative material system. If device dimensions from production lines reduce in size by the same rate as present, soon 0.1 μm devices will be realised on production lines. Questions still remain about whether optical lithography and MOSFETs can be economically and technically scaled to 0.1 μm and below.

It would be advantageous to find a new option compatible with existing Si based technology that could utilise the economics of Si and the vast automated knowledge that depends on its unique properties. One approach is to try and

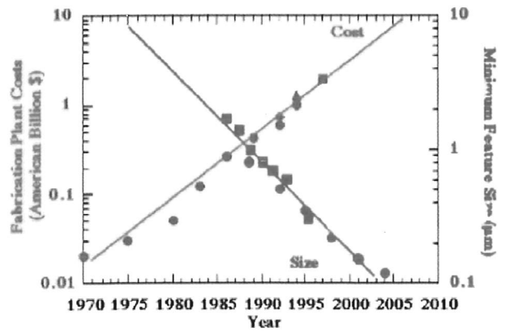

Figure 1.1: This shows the increase in manufacturing plant fabrication costs and Reduction in minimum feature size per year [5].

find an alternative compatible material system that will allow the production of devices with a higher performance of functionality [7]. Silicon/silicon-germanium (Si/SiGe) heterostructures have been suggested as one possible method for increasing device performance at small dimensions and solving a number of problems encountered in MOSFET structures [8]. Theoretical modelling has predicted significant advantages in using Si/SiGe modulation-doped field effect transistors (MODFETs) for sub-0.25 μm devices [9, 10] and experimentally demonstrated performance is impressive [11, 12].

1.3 Silicon-Germanium on Si Material systems

Extensive research has been carried out into alternative and more exotic materials systems, different to Si such as group III-V and some II-VI materials. Whilst some III-V materials such as GaAs/AlGaAs have demonstrated consistently superior electronic properties, they have failed to replace Si as the dominant semiconductor, due to the higher wafer production and fabrication costs and the massive capital expenditure required to change to a III-V based manufacturing system.

Silicon-germanium (SiGe) attempts to bridge the gap between Si and more elaborate material systems by providing a semiconductor material that has better performance than Si, can utilise some of the better material properties of Si but remains cheaper than III-V materials. There are many applications where the introduction of SiGe into a Si device can offer enhanced performance for only a relatively small increase in cost. This improved device performance has led to a great deal of research and investment in the SiGe system [13].

Si/SiGe heterostructures offer the possibility of improving standard Si bipolar device performance engineering and is the most rapidly expanding areas in Si-based integrated electronics. It is driven by exponential market growth for a wide variety of consumer wireless products (including mobile phones, mobile computing devices, global positioning systems).

Recent success in incorporating Ge into Si bipolar transistors has now enabled Si to be used in frequency ranges in which only more expensive semiconductor technologies, such as GaAs, could previously be used. The ability to use Si based technologies in these frequency ranges will enable the mass production of a large variety of sophisticated high frequency wireless integrated products. SiGe is particularly useful in high-frequency, low-noise applications, and has the additional advantage of still being compatible with the conventional mainstream Si technology. SiGe microstructures can also enable the integration of optical devices (LED's and photodiodes) with Si based conventional integrated circuits (although these are only at a research stage).

For high performance SiGe modulation-doped field effect transistors (MODFETs), a tensile strained-Si quantum well must be grown on a substrate with a lattice constant of approximately cubic $Si_{1-x}Ge_x$ alloy $0.2 < x < 0.4$ [14, 15]. Impressive room temperature mobilities have been demonstrated by modulation-doped 2DEGs [15] and 2DHGs [16] on SiGe virtual substrates, while the pseudomorphic SiGe channel devices have shown relatively poor performance [17].

At low temperatures, electron mobilities in virtual substrate 2DEGs have reached values up to 390 000 $cm^2V^{-1}s^{-1}$ at 400 mK [18]. Virtual substrate 2DHGs display mobilities of 55 000 $cm^2V^{-1}s^{-1}$ at 4.2 K [19], while the pseudomorphic 2DHGs in the metallic regime have only reached 20 000 $cm^2V^{-1}s^{-1}$ at low temperatures [20]. Clearly the high performance SiGe MODFET or MOS devices are those fabricated using the virtual substrate technology [11,21].

SiGe is also of importance in the research of low dimensional physical systems (see Section 2.1.2) since it provides an alternative material system to test the validity of certain theories. There is strain associated with the introduction of Ge into a Si structure (discussed in detail in Section 1.4). The strain in the system is dependant on the Ge concentration and so it is possible to control the strain in a Si/SiGe heterostructure. Varying the strain and Ge content will alter the bandgap, effective mass (m^*) and band alignments, a technique commonly known as bandgap engineering.

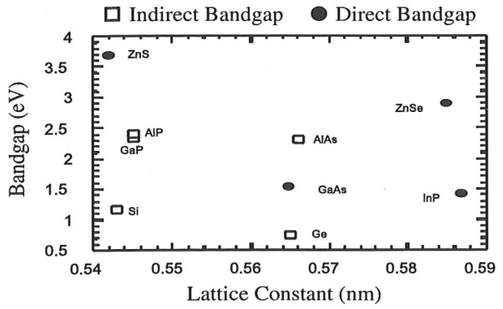

Figure 1.2: Lattice constants and bandgap for various semiconductors. This figure shows the bandgap energy for some of the more common direct and indirect bandgap semiconductors.

SiGe has certain material properties that differentiate it from materials such as GaAs/AlGaAs and so the use of SiGe may give rise to effects that have not been previously observed. Important differences between Si/SiGe and GaAs/AlGaAs include the indirect bandgap, strained layers, conduction band valley-degeneracy and differing effective electron and hole masses (discussed in Section 1.6).

If two different materials are to be successfully combined then both materials will need to have matched lattice constants in order to avoid forming defects due to interfaces. Figure 1.2 shows the lattice constants as well as the bandgap energy for various indirect bandgap and direct bandgap semiconductors. Si and Ge have the same crystal structure and both have an indirect bandgap. Ge has an atomic spacing that is 4.2% greater than that of Si. Figure 1.3 shows schematically that SiGe will have a larger lattice constant than pure Si and so it is difficult to grow thick layers of SiGe directly on Si without producing any defects.

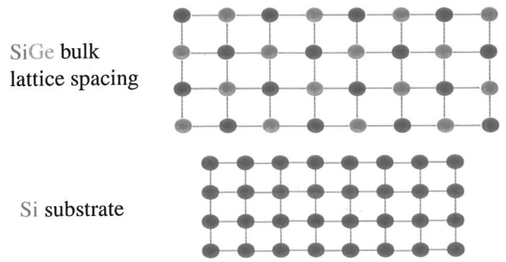

Figure 1.3: Bulk SiGe and Si lattice structures

1.4 Strained Silicon-Germanium Layer Growth

When a thin layer of Ge atoms is deposited on to a much thicker Si substrate, instead of expanding to their normal size they are locked in place by the underlying Si. The layer of Ge experiences a lot of strain that increases as the layers of Ge accumulate. Ultimately defects occur to relieve the strain and entire rows of Ge atoms squeeze out of the lattice, allowing the remaining Ge atoms in the layer to move apart from one another. In order to have a fully relaxed structure, 4 out of every 100 Ge atoms grown along a Si/Ge interface will only have 3 bonded neighbours and the remaining 'dangling' bond can serve as a site for carrier generation or recombination, seriously degrading the electronic properties.

It would seem that this mismatch might cause insurmountable problems, but even when semiconductor research was in its infancy in 1949, it was suggested that it might be possible to grow a strained layer of one material on another without causing a very large number of misfit dislocations [22]. Heteroepitaxy of semiconductors with different lattice constants is limited to a certain critical thickness up to which the mismatch is accommodated by strain [23], as shown in Figure 1.4a. Above this critical thickness, the strain will be relaxed by the formation of misfit dislocations, as shown in Figure 1.4b. As the thickness of the alloy increases, the reduction in dangling-bond energy is overwhelmed by the increased strain caused by the accumulating layers. When this eventually occurs the alloy will reorder to its undistorted arrangement, forming rows of interfacial dangling bonds [24].

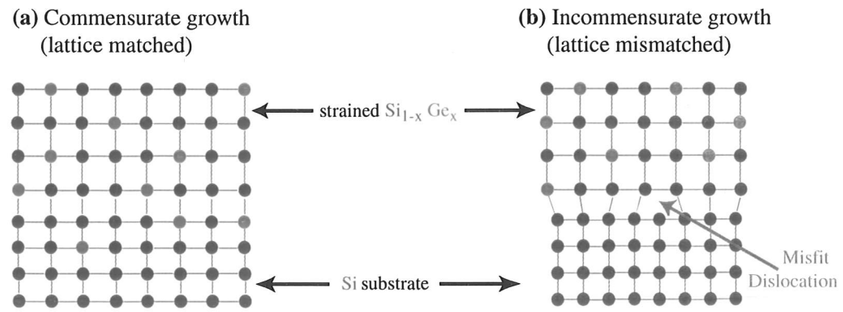

Figure 1.4: (a) Commensurate (lattice matched) growth of SiGe on Si lattice structures. (b) Incommensurate (lattice mismatched) growth of SiGe on Si lattice structures.

1.4.1 Growth of SiGe on Si

If a thick SiGe layer is grown directly on a Si lattice it will give incommensurate (lattice mismatched) growth as shown in figure 1.4b. The resulting mismatched lattices will cause misfit dislocations that act to relieve the strain. These dislocations can thread their way through the wafer and ruin device performance. The epilayer is said to relax and the defects significantly reduce the mobility and electronic quality of the material [25].

For many applications it is necessary to produce low defect density, relaxed SiGe on a Si substrate. As long as the SiGe layer is thin enough then the first few atomic planes will compress in the growth plane to match the smaller crystal lattice spacing of the substrate crystals as shown in Figure 1.4a. The strain energy is the lowest energy configuration and the re-ordering process involves gross atomic rearrangement - effectively providing an energy barrier. This commensurate growth (lattice matched) is stable as long as the energy due to the strain is less than that which would result from dislocations.

1.4.2 Critical Thickness

Van der Merwe was the first to calculate the critical conditions for the number of misfits that could be tolerated before the onset of dislocations [26]. Since then numerous models have been developed to predict the critical thickness, h_{crit}. The critical thickness is dependent on factors such as the percentage of Ge, x, in the $Si_{1-x}Ge_x$ and the temperature and time of substrate growth [27]. The areal energy density, ξ_h, due to compressive strain can be given by:

$$\xi_h = 2g\frac{1+\nu}{1-\nu}he^2_{in-plane} \tag{1.1}$$

where h is the layer thickness, g is the shear modulus, ν is Poisson ratio and $e_{in-plane}$ is the in-plane stress component [26]. The strain in a layer of the heterostructure is:

$$e^2_{in-plane} = \frac{a_s - a_i}{a_i} \tag{1.2}$$

where a_s is the substrate lattice constant and a_i is the layer lattice constant. The most common values that are quoted come from the model of Matthews and Blakeslee [23] who used an approach based on balancing the tension in a

dislocation against the force due to misfit strain. This gives rise to a critical thickness of:

$$h_c = \left(\frac{a_o}{f_o\sqrt{2}}\right)\frac{1-\nu\cos^2\Theta}{1-\nu}\left(1+\ln\frac{h_c\sqrt{2}}{a_o}\right) \tag{1.3}$$

where f_o is the misfit density between the substrate and epilayer, a_o is the bulk lattice parameter of the epilayer and Θ is the angle of the dislocation. Matthews and Blakeslee[23] calculated the critical thickness in terms of the Ge fraction (x) as:

$$h_{crit} \cong \frac{0.55}{x}ln(10h_{crit})nm \tag{1.4}$$

A good fit to Equation 1.4 has been given by Dr. D. J. Paul [2], explicitly relating the Ge fraction to the critical thickness:

$$h_{crit} \cong 1.7993(x^{-1.2371})nm \tag{1.5}$$

The rate at which strain is relieved, after misfit dislocation occurs, is then dependent on the multiplication and propagation of the dislocation segment. Specifically for the SiGe system, measurements show threading dislocations velocities to follow the empirical expression [28]:

$$v = A\tau^m e^{\frac{-U}{kT}} \tag{1.6}$$

for a given temperature T, where A is a constant, m an exponent ~ 1.1, for the resolved shear stress τ and U is the activation energy.

One idea for growing thick strained SiGe layers is to grow strained layers up to the critical thickness and then to cap the structure with a thin layer of the same lattice constant before growing another layer of identical composition as the first [26]. Houghton, who produced a semi-empirical kinetic model calculating h_{crit} for strained SiGe layers grown pseudomorphically on bulk Si(100) substrates [27], showed that a cap of the same composition as the substrate does not effectively protect the strained layer from relaxation. This is due to the cancellation of the strain fields of the dislocation pairs that have been produced.

In reality it is frequently observed that layers significantly thicker than h_{crit} can be grown with no signs of relaxation [29]. This is mainly attributed to the formation of a metastable layer, which provides a kinetic barrier to the nucleation and propagation of misfit dislocations. In order to form a dislocation atomic

[2] *private communication*

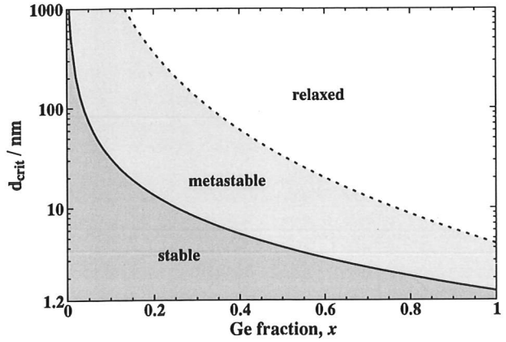

Figure 1.5: Equilibrium and metastable critical thicknesses for SiGe on Si(100). These are approximate curves for growth at 550°C and vary with growth conditions. The stable and metastable growth regimes are shown as the shaded region.

readjustment kinetic energy is necessary which acts as an activation barrier. In the metastable region, the potential energy due to strain exceeds that required to form a dislocation, although there is insufficient energy to overcome the activation barrier. This was first modelled by Dodson and Tsao [30] who considered activated propagation and nucleation of pre-existing dislocations. In the metastable region, thermal excitation can lead to lattice relaxation and hence a great deal of care needs to be exercised with high temperature processes. Figure 1.5 shows the equilibrium and metastable critical thickness for SiGe on Si(100). There are approximate curves for growth at 550°C and these curves can vary with growth conditions.

1.5 SiGe Virtual Substrates

While it is possible to make SiGe wafers [31], they do not compare favourably with the quality of Si wafers. SiGe crystals can be obtained from Russian sources as well as Virginia Wafer Tech. However a common defect is that the Ge clusters together, so that the concentration varies within the crystal and as a result, industrial companies tend not to favour such systems. For a high yield and good device performance there should be a low density of threading dislocations ($< 10^6$ cm^{-2}) and smooth surfaces (r.m.s. surface roughness smaller than 2 nm). Ideally there should also be sufficiently high carrier transport mobility in the strained structure deposited on the top of the SiGe buffer.

Since relaxed SiGe substrates with the bulk lattice constant of SiGe cannot be grown directly at present, the solution has been to grow a SiGe 'virtual substrate' on an existing Si substrate. A virtual substrate refers to a thick layer of high quality relaxed SiGe on a standard Si substrate, on top of which strained Si, Ge or normal SiGe can be grown [14, 15]. It was not until the mid-1970s that the first attempts were made to grow pseudomorphic SiGe on a Si substrate [32, 33] and further progress occurred in the 1980's where improved quality layers were produced [29, 34].

The simplest method for growing a relaxed SiGe layer on a Si substrate consists of growing a thick SiGe alloy layer which greatly exceeds the critical thickness. The strain is constant throughout the layer and strain energy builds up as the layer thickness increases, until relaxation occurs. The residual strain within the layer gradually decreases by misfit dislocation generation as the layer thickness increases. This results in an extremely high density of dislocations, greater than 10^9 cm^{-2} [35]. The high density occurs because the strain relaxing misfit dislocation segments interact to pin each other, which prevents them from extending. Each misfit segment is associated with pair of dislocations that thread upwards through the active layers and give enormous surface densities of dislocations, around 10^{12} cm^{-2} [14] that will severely impair device performance and so significantly effect device yields from wafers, making them uneconomic.

A stepped composition buffer where a step is grown and then annealed at greater than 1000°C, allows equilibrium conditions after each step, so there is a low threading dislocation density [36]. Such buffers take days to grow. It has been shown that by slowly grading the Ge content across the buffer region during growth, the final quality of the material will have improved, since it helps filter out the dislocations [35].

In order to minimize the number of dislocations in the strain relaxed sections, large SiGe graded 'buffer' layers are used. Tersoff and Beanland *et al.* have developed theories to describe the graded virtual substrate [37, 38]. In graded layers the strain is gradually increased, which leads to a uniform generation of dislocations within the layer, so that the number and density of dislocations can be controlled. This has a significant advantage in reducing the number of threading dislocations.

Misfits can be spread through the buffer region and so they interact less. Hence there is a much lower density of threading dislocations at the surface

[14, 39]. Misfit segments are almost entirely confined to the graded layers, well away from the active layers and can even penetrate down into the Si substrate, as a result of multiplication by a Frank-Read mechanism [40]. Many defects will glide to the edge of the wafer or are mutually compensated by dislocations caused from self-aligned sources [41], a technique which is used to improve the quality of the wafers.

Since a certain thickness of material is always required to produce a new dislocation within the graded structure, it follows that at the surface of the grade there will be a region which is free of misfit dislocations. It is common to cap this region with a layer of uniform composition which is also dislocation free. This procedure leads to high density of misfit dislocations close to the substrate, but the density of threading dislocations in the top layers is significantly reduced (down to $\sim 10^5$ cm^{-2}) [42].

The Ge fraction, x, in the $Si_{1-x}Ge_x$ graded region is increased until the desired value is reached, across a certain distance. The initial fraction is normally very low and in most wafers used in the course of this thesis, the virtual substrates are graded from $x = 0$ to around $x = 0.23$. The graded buffer layers, which are grown as intermediate epitaxial layers between the Si substrate and the active heterostructures, are designed to maximise the length of the misfit segments so that fewer threading dislocations are required to relax the strain.

Figure 1.6 shows a schematic of a SiGe virtual substrate grown on a Si(100) substrate. This figure shows that the misfits and threading dislocations are to be confined to the graded buffer regions. Grading gives rise to gradual strain relaxation throughout the region with dislocations forming at the base of each relaxation process. Threading of dislocations upwards into the doped regions does not occur with as high a rate as downwards or towards the wafer edge [39].

Graded layers give poor surface morphology compared to bulk Si and show a characteristic cross-hatch pattern along the <110> direction, which correspond to the intersection of the {111} dislocation-glide planes with the (100) surface that is commonly used for most structures. The cross-hatch patterns have a small period of only a few μm and their initial formation may result from atomic steps due to dislocation glide [43] and from the inhomogeneous strain field caused by underlying misfit segments [44].

Shallow pits are another common surface feature which arise from a strain field caused by threading dislocations [45]. These form in order to minimize the

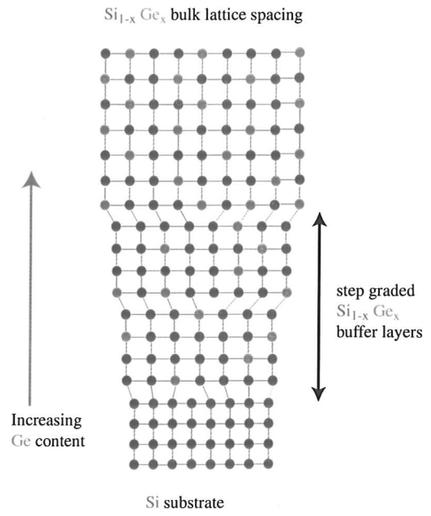

Figure 1.6: A schematic of a SiGe virtual substrate grown on a Si(100) substrate. This figure shows that the misfits and threading dislocations are to be confined to the graded buffer regions. A bulk SiGe with the desired Ge fraction, x, can be grown with a low defect density.

energy associated with threading dislocations, by reducing their length. It is uncommon for many threading dislocations to form large pitted structures. Low temperature growth helps to reduce surface morphology problems but is not as effective in promoting dislocation propagation in the buffer layers. It is possible to enhance surface morphology by using slow grading rates but since these will require a very thick buffer it will take much longer to grow. Nearly perfect lattice relaxation occurs during growth, due to the high substrate temperature (greater than 750°C) and the slow increase of the Ge concentration.

1.6 Band Structure

The strain present in lattice-mismatched Si/SiGe heterostructures can be used as a tool for band structure engineering both to improve device performance and offer new functionality [13, 14, 39, 46, 47, 48]. The band structure has a great deal of importance and there are many papers that cover band structure and related properties (such as [49, 50]). Given the extremely broad and complex combination of factors such as different alloy compositions and strain conditions, only a brief overview of structures presented in this thesis is given here.

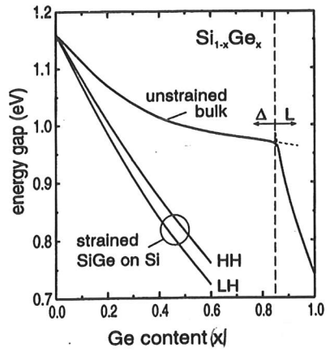

Figure 1.7: The variation of the low temperature fundamental bandgaps for bulk unstrained $Si_{1-x}Ge_x$ and strained $Si_{1-x}Ge_x$ grown on bulk relaxed Si as a function on the Ge fraction, x for Light Holes (LH) and Heavy Holes (HH) [51]. At approximately $x = 0.85$, the band structure changes from Si-like to Ge-like.

1.6.1 Bandgap

The valence band minima for both Si and Ge is at the Γ point (the origin of momentum space) but the conduction band (CB) minima of both Si and Ge are offset and are not at the centre of the Brillouin Zone (BZ). One consequence of this is that any electron-hole recombination in Si or Ge requires a change in momentum. Figure 1.2 shows that Ge has a smaller fundamental bandgap than Si. In a SiGe alloy, the fundamental bandgap energy varies with composition for bulk structures.

The symmetry of the cubic crystal means that there are a number of energy-degenerate CB minima. In Ge there is an eight-fold degeneracy with the minima directed along the L-points (the <111> direction) and are at the BZ boundary. In Si there is a six-fold degeneracy with the minima directed along the Δ-points (the <100> direction) and are at 85% of the distance to the Brillouin zone boundary.

Figure 1.7 shows the variation of the low temperature fundamental bandgaps for bulk unstrained $Si_{1-x}Ge_x$ and strained $Si_{1-x}Ge_x$ grown on bulk Si as a function of the Ge fraction, x [51]. At approximately $x = 0.85$, the band structure changes from Si-like to Ge-like. The difference in the symmetry of the CB minima means that there is a discontinuity in the bandgap at $x = 0.85$ for bulk $Si_{1-x}Ge_x$. When $x < 0.85$, Δ-valleys define the minima since these are lower in energy. However if $x > 0.85$ the L-valleys are lowest in energy. This is shown in Figure 1.7. All of the $Si/Si_{1-x}Ge_x$ structures used in this thesis have $x < 0.85$.

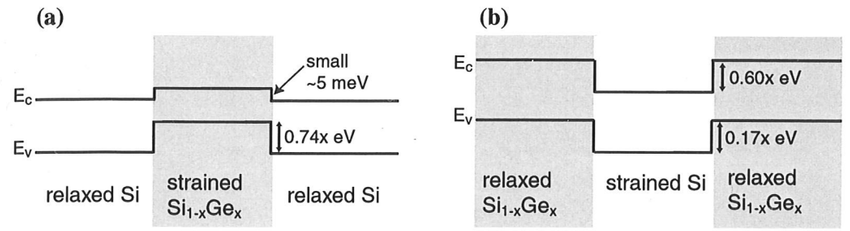

Figure 1.8: Band offsets in $Si/Si_{1-x}Ge_x$ heterostructures; (a) shows strained SiGe grown on relaxed Si and (b) shows strained Si grown on relaxed SiGe.

The constant energy surfaces in momentum space close to the CB minima have elliptical shapes, resulting in unequal effective masses in different directions. The constant energy surface in momentum space close to the CB minima is shown in Figure 1.10b. The effective mass, m^*, which describes how the particles respond to an applied force can be calculated using

$$m^* = \hbar^2 \left(\frac{d^2 E(k)}{dk^2} \right)^{-1} \quad (1)$$

where $\hbar$ is Planck's constant divided by 2π. This is defined in terms of the momentum-energy dispersion. Si has two different values for m^* for electrons; m^*=0.196m_e in directions parallel to the long axis and $m^* = 0.91\ m_e$ in directions normal to this (where m_e is the mass of an electron). Δ-valleys in bulk SiGe are expected to behave similarly [49].

1.6.2 Band Alignment

In order to produce either a 2DEG or 2DHG requires a quantum well in heterostructure with considerable discontinuity at the Si and SiGe interface. The conduction band offset is negligibly small for pseudomorphically grown SiGe on Si whereas the valence band edges are higher in SiGe compared to Si (see Figure 1.8). Therefore electrons do not experience a potential barrier on crossing the Si/SiGe interface. The valence band edges are always higher in SiGe compared to Si, regardless of the strain conditions. The valence band discontinuity, ΔE_v, given by Reiger and Vogl [49] is:

$$\Delta E_v = (0.74 - 0.53x_s)(x - x_s) \quad (1.8)$$

where x_s is the Ge concentration in the bulk substrate.

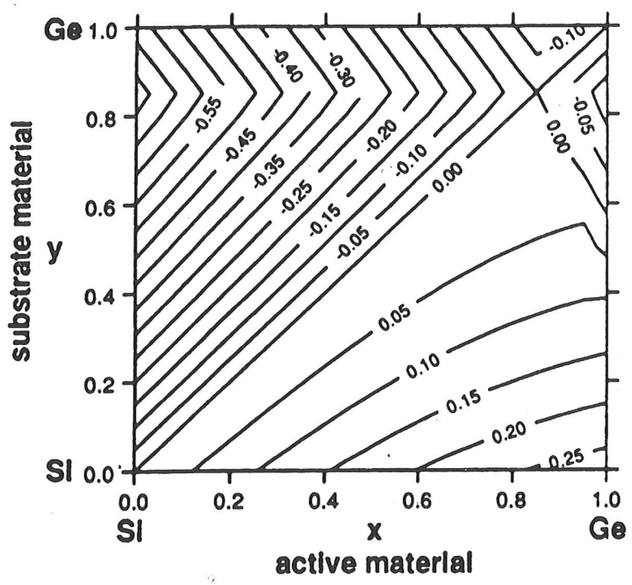

Figure 1.9: The conduction band offsets in SiGe heterostructures [49].

This formula is valid for all x ranges and the active region in simple heterostructures can be experimentally found using capacitance-voltage profiling [52]. Calculations by Reiger and Vogl [49] suggested that the band structure of Si/SiGe would have a type II alignment [35] for almost all compositions *i.e.* the conduction and valence band offsets are in the same direction and this has been verified experimentally [53].

If the whole structure is forced to take the in-plane lattice constant of the SiGe layer instead of that of Si, a large offset appears in the CB, though the valence band offset is somewhat reduced, as depicted in Figure 1.8. This phenomenon was first suggested by Abstreiter *et al.* [54], to explain the fact that it was possible to confine electrons in layers of Si on relaxed SiGe.

Calculations to verify this band structure were performed soon thereafter by People and Bean [55]. Since the CB offset is quite small, the value can be extrapolated from the bandgap difference and the valence band offsets between the two material. Values for the CB offset have been calculated by Reiger and Vogl [49] and are shown in Figure 1.9.

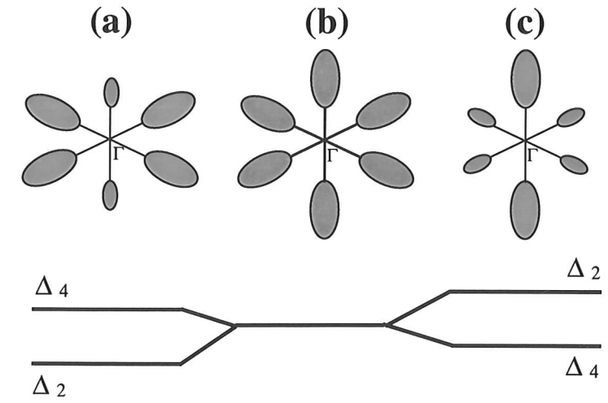

Figure 1.10: The conduction band minima in Si. The constant-energy surfaces for the CB minima are also shown; (a) is the CB minima for compressively strained SiGe on Si, (b) is the CB minima for bulk Si and (c) is the CB minima for strained Si on relaxed SiGe.

1.6.3 Effects of Strains

It has been shown that strain can alter the alignment of the band edges, but this is only one consequence of the rearrangement of energy levels which occurs. The tight binding model used to calculate the band structure of the material depends on the overlap of atomic wavefunctions for neighbouring atoms. If the atomic distribution is altered, through strain, there is a different overlap of atomic orbitals and the energy of the valence and conduction bands will be altered. The conduction band minima are shifted and there is a change in the constant energy surface for the CB minima as shown in Figure 1.10

The strain experienced by the layers can be broken down into two components. An overall shift in energy of each of the bands, changing their relative positions is caused by hydrostatic strain, which gives a volume change of the unit cell. A biaxial component to the strain, which is compressive for SiGe channels and tensile for Si channels, causes tetragonal distortion of the cubic lattice. The reduction in symmetry changes the energy level structure within the bands, lifting the six-fold valley degeneracy in the CB and the degeneracy between the light-hole (LH) and heavy-hole (HH) bands which exists at $\mathbf{k} = 0$ in the valence band. The spin-orbit (SO) split-off band also increases its energy separation from the valence band edge.

For strained Si on SiGe, the in-plane lattice constant increases and the in-

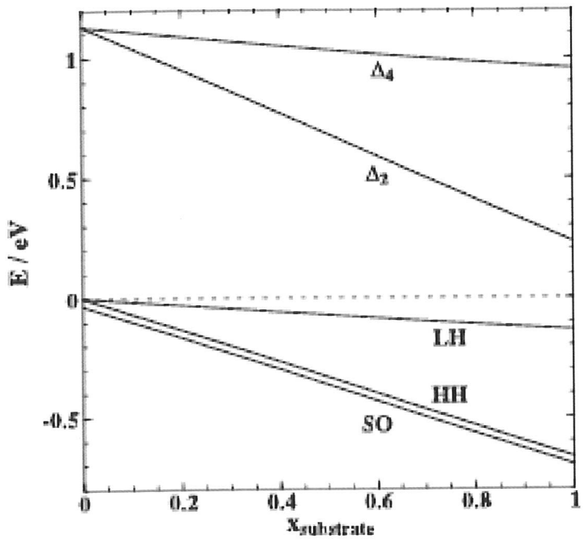

Figure 1.11: The calculated energy-level shifts in the CB and VB as a function of the Ge fraction, x, for strained Si on a relaxed $Si_{1-x}Ge_x$ substrate [47].

plane reciprocal lattice vector decreases in magnitude and the CB minima lie closer to the BZ centre. This will increase the perturbation due to adjacent atoms in this direction and consequently the energy of these levels decreases. This breaks the 6-fold symmetry and the Δ_2 energy states are lower in energy than the in-plane Δ_4 as shown in figure 1.11.

Bands in the 2DEG structures become simplified since only the two lowered-energy valleys will normally be occupied. As electrons are confined to two dimensions, transport in the plane is only affected by the small, in-plane effective mass. Since there are no other bands with similar energy and wavevector that might distort the band dispersions, these valleys should be fairly parabolic and so have an energy-independent effective mass (from Equation 1.7). The perpendicular effective mass only affects the degree of confinement. Since this mass is large, the zero-point energy will be small, leading to stronger confinement.

For compressively strained SiGe alloys on Si, the in-plane lattice constant decreases. This increases the perturbations felt by the Δ_4 states due to adjacent atoms, which reduces the energy of these levels and so the CB minima lie further away from the BZ centre. The Δ_2 levels increase in energy as the lattice constant in the growth direction increases and the six-fold degeneracy is broken. The Δ_4

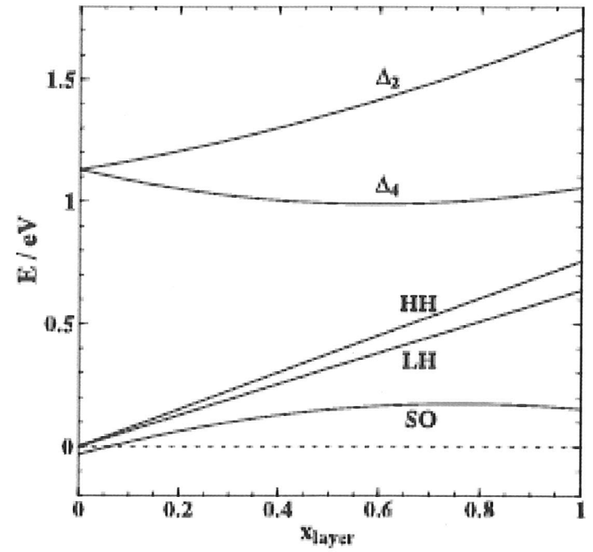

Figure 1.12: The calculated energy-level shifts in the CB and VB as a function of the Ge fraction, x, for strained $Si_{1-x}Ge_x$ on a relaxed Si substrate [47].

energy states have a lower energy than the Δ_2 energy states as shown in figure 1.12. In addition the effective mass becomes directionally dependent due to the asymmetric potential caused by the strain.

Si and Ge both have a valence band maxima at the BZ centre. There is six-fold degeneracy in energy with three bands, LH [J = $(\frac{3}{2}, \frac{1}{2})$], HH [J = $(\frac{3}{2}, \frac{1}{2})$] and SO split off [J = $(\frac{1}{2}, \frac{1}{2})$] degenerate in energy. Despite the lack of valley degeneracy, valence bands tend to be more complicated because of the orbital component of angular momentum in these bands. This results in total angular momentum of J = $\frac{1}{2}$ in the SO split-off band ($m_j = \pm\frac{1}{2}$) and J = $\frac{3}{2}$ in the remaining bands: $m_j = \pm\frac{1}{2}$ in the LH band and $m_j = \pm\frac{3}{2}$ in the HH band. The proximity of these different levels causes them to interact, leading to distorted band profiles.

The application of strain gives rise to coupling between the J = $\frac{1}{2}$ and J = $\frac{3}{2}$ states, which leads to the loss of six-fold degeneracy. The effect of strain on the valence band in strained Si on SiGe, is to cause the LH band to have a greater energy than the HH band. The opposite of this occurs with strained SiGe on Si, with HH band being higher in energy than the LH band. The spreading out in energy of the LH, HH and SO bands as a result of the strain, means that the band distortion is significantly reduced, especially near the valence band edge,

where only one band is occupied. When there are low carrier densities the band is approximately parabolic, whereas at high densities mixing with other bands results in non-parabolicities [56], and also anisotropies [56, 57] in the dispersion relation. This makes it very difficult to calculate the effective mass, which is now directionally dependent, as discussed in [58].

1.7 Electrical Properties of SiGe

In order to allow SiGe to conduct electricity, impurities which enhance the mobile electron (or hole) concentration called *dopants*, are introduced intentionally (and unintentionally) during semiconductor growth. Impurity atoms incorporated in a SiGe lattice take up either Si or Ge sites and can form donors or acceptors. Donor impurities such as arsenic, As or phosphorous, P, have an excess of valence electrons that are free and mobile for current conduction. Acceptors impurities such as boron, B, which are short of electrons, leave free holes. The introduction of a small amount of donor or acceptor atoms (as little as 1 in $1{\times}10^7$) into a semiconductor material will reduce the resistivity by several orders of magnitude.

The band discontinuity that exists at the abrupt Si/SiGe heterointerface allows the formation of two dimensional electron gases (2DEGs) or two dimensional hole gases (2DHGs), depending on the type of dopant used. Modulation-doping involves doping a semiconductor in a region separated from the Si quantum well and so ionised donors are spatially separated from the 2D gas at the heterojunction. Typical modulation-doped 2DEG and 2DHG structures are shown schematically in chapter four.

Physical separation of charged carriers from parent atoms allows very high mobilities to be achieved, especially at low temperatures. In this case phonon scattering is negligible and ionised impurity scattering tends to be the dominant mobility limiting mechanism in modulation-doped heterostructures. In extreme cases background impurity scattering is the dominant scattering mechanism but this only occurs in the very highest mobility samples. Remote ionised impurity scattering tends to be the limiting scattering mechanism at low temperatures and this can be reduced by increasing the distance between the doped SiGe layer and the heterointerface. However, as the spacer layer thickness increases, the efficiency of carrier transfer from the donor layer into the 2D gas is reduced. An optimal separation has to be reached between high mobilities and sufficient

population of the 2D gas itself. This is further investigated in chapters four, five and six.

The carrier concentration of a 2D gas can be enhanced by liberating any carriers that exist in deep traps in the SiGe layer. These traps are too deep for the carriers to be liberated by thermal energy alone [59]. Illumination with a red light emitting diode (LED) is used to photo-excite these carriers into the 2D gas. Since the heterointerface barrier is greater than the thermal energy of the carriers, population enhancement of the 2D gas persists after illumination stops. This effect is called persistent photoconductivity or PPC [60]. An enhanced carrier concentration produces an increase in mobility as the increased electron-electron interaction screens the Coulomb potential from the remote ionised impurities. The mobility will increase until the carrier concentration starts to occupy the second sub-band at which point the mobility drops. For most samples described in this thesis, the confinement is sufficiently strong that only the first 2D sub-band will be occupied at the carrier densities that have been obtained.

The application of a bias to a surface Schottky gate can also be used to vary the carrier concentration in a modulation-doped device. A Schottky gate refers to the rectifying barrier formed when a metal (eg Au) is in intimate contact with a semiconductor surface. Voltage biases can be applied to change the band-profile of the semiconductor. In the case of a 2DEG, the application of a negative bias raises the barrier and produces a shallower well at the interface, thus confining fewer carriers in the 2DEG. Conversely, by applying a positive bias, the well can be deepened and the 2DEG carrier concentration, increased. The magnitude of the applied voltage is limited by the occurrence of leakage currents between the 2DEG and gate. Gated modulation n-type doped heterostructures are sometimes referred to as High Electron Mobility Transistors (HEMTs).

Chapter Summary

This chapter provided a brief review on the background of SiGe based heterostructures. The uses of SiGe on Si devices is covered and there is also a summary of the material and electrical properties of Si/SiGe heterostructures.

Chapter 2

Two Dimensional Transport Theory

In this chapter a brief description of transport properties of 2D gases is given. The main focus is on 2DEGs, but most of the equations presented here also apply equally well to 2DHGs (with an appropriate change of sign and effective mass). There is a brief outline of some of the basic concepts on the transport of charge carriers in different regimes, such as in electric or magnetic fields. A detailed analysis of transport theory can be found in references [61, 62].

2.1 Reduced-Dimensional Systems and Length Scales

2.1.1 Reduced Dimensional Structures

In bulk metals and semiconductors, electrons (or holes) are normally free to move in all three spatial directions. If there is a restriction on this freedom in certain directions, then the dimensionality of the system is reduced. In a two dimensional (2D) system the electrons can only move in one plane and may not travel perpendicular to this plane. An example of a naturally occurring material showing quasi-2D behaviour is graphite where the resistance measured along the sheets is much lower than between sheets. In the 2D semiconductor systems found in MOSFETs, heterojunctions and quantum wells the electron motion is confined to a single plane and it is possible to control the actual position and density of the charges with surface gates. This forms the basis of most of the Si electronics industry.

As well as confining the position of a particle, reducing the dimensions also

changes the allowed energy levels, since the available momentum states are restricted. One dimensional (1D) systems where motion is only along a line, also occur naturally, examples of which are transport along a polymer chain. 1D systems have been fabricated in semiconductors by advanced lithography techniques where they are known as quantum wires. If confinement occurs in 3D then a zero dimensional (0D) system is formed. Fabricated 0D systems in semiconductors are called quantum dots, the natural version being an atom.

In a reduced dimensional system it is possible to experimentally detect the effects of quantum confinement. It is important to decide which microscopic length scales are important in determining the dimensionality of a system. In a quantum mechanically confined system the finite width in the confinement direction can usually be ignored. However in some cases this width is important and less confined systems may behave as if they have reduced dimensionality. Some of the more important scattering and characteristic length scales are given below. It is assumed that the sample has a length **L**, width **W** and thickness **t**. For more information on reduced dimensional systems see [61].

2.1.2 Length Scales

In most conduction processes in semiconductors only electrons near the Fermi energy, $\mathbf{E_F}$, need to be considered for which the relevant length scale is the Fermi wavelength, λ_F.

The Fermi wavelength arises from the quantum mechanical behaviour of the electrons in a confined system. An important aspect of this behaviour is the Pauli exclusion principle, which states that no two half-spin particles (*i.e.* fermions such as electrons) may occupy the same state. Consequently the electrons will minimize the total energy of the system and will occupy all of the states available up to a well defined Fermi Energy, $\mathbf{E_F}$, which varies with the number of electrons.

Fermi wavelength, λ_F, and the Fermi Energy, $\mathbf{E_F}$

$\mathbf{E_F}$ is related to λ_F by: $\lambda_F = \frac{2\pi}{\mathbf{k_F}} = \sqrt{\frac{2\pi}{\mathbf{n_s}}} = \frac{\mathbf{h}}{\sqrt{2\mathbf{m^* E_F}}}$, where $\mathbf{n_s}$ is the sheet carrier concentration and **h** is Planck's constant.

The states that can be occupied by an electron are well determined because they are described by a wavefunction. In a sample with thickness W, to satisfy periodic boundary conditions the wavefunction must have a wavelength λ=W/n for an integer n (this applies to the wavelength component along each axis).

The energy of a state E is proportional to λ^{-2} and so if the width W is reduced then the energy of all of the states is increased. Electrons at the Fermi energy $\mathbf{E_F}$ have a wavelength $\lambda_\mathbf{F}$ and so only states where the wavelength $\lambda \geq \lambda_\mathbf{F}$ will be occupied. If W is reduced to less than $2\lambda_\mathbf{F}$, only states with n = 1 can be populated. Here only the first 2D sub-band is occupied, since the states occupy a band of energies, but with wavevectors that differ only by their components in the plane. Such a system is a 2-dimensional electron gas (2DEG). Confining carriers in the valence band of the semiconductor produces a 2DHG. Higher 2D sub-bands can be occupied if the thickness is larger or if there is a larger $\mathbf{E_F}$ (due to a higher density of holes). If only a few sub-bands are occupied then the system is said to be quasi-2D.

At high temperatures the conductivity of a 2DEG or 2DHG is well described by the Boltzmann expression for conductivity:

$$\sigma_B = \frac{\mathbf{n_s e^2} \tau_t}{\mathbf{m^*}} \tag{2.1}$$

where e is the electronic charge, $\mathbf{m^*}$ is the electron effective mass and τ_t is the elastic scattering lifetime.

At lower temperatures there are significant corrections to the Boltzmann conductivity due to effects such as disorder, electron-electron interactions, quantum interference and ballistic transport. By measuring changes to the Boltzmann conductivity as functions of temperature and magnetic fields, the appropriate corrections can be determined and used to extract information about the inelastic processes in the system.

Scattering lengths

Scattering length scales (especially the mean free path, l) are very important and can be compared to size of the sample in order to define a number of different transport regimes.

The relationship between any scattering length l_x and its equivalent scattering time τ_x is defined by the diffusion constant, D (in a general time-scale $\tau_x >> \tau_t$):

$$l_x = \sqrt{D\tau_x} \tag{2.2}$$

The electron transport mobility μ is defined as $\mu = \frac{\mathbf{m^* e}}{\tau}$.

The diffusion constant D is related to μ for an absolute temperature T, by the Einstein relation: $\mu = \frac{eD}{k_B T}$ where k_B is the Boltzmann constant.

The **inelastic scattering length**, $l_{\mathbf{in}}$, is the distance an electron travels with constant kinetic energy. Energy changing collisions include those with other electrons (at low temperature) and collisions with phonons, which become more important at higher temperatures.

The **elastic scattering length**, $l_{\mathbf{el}}$, is the distance an electron travels with a constant wave vector. This is determined by scattering events involving fixed potential fluctuations in the lattice. The effects from Coulomb impurity potentials are an example of elastic scattering.

The **mean free path**, $l = \mathbf{v_F}\tau_\mathbf{t}$, is the minimum of the elastic and inelastic scattering lengths and is the distance over which the initial momentum of a particle is lost as a result of scattering. In most semiconductor systems the mean free path is the shortest scattering length.

The **phase coherence length**, l_ϕ, is the distance that an electron will travel and retain its phase coherence. This can be used to generally determine how far an electron can travel and still be affected by quantum interference.

Length Scales associated with Physical Quantities

As well as the scattering lengths, it is also important to consider length scales that are associated with physical quantities, such as temperature, magnetic field and electric field.

The magnetic field, **B**, produces a characteristic length scale, the **magnetic length**, $l_B = \sqrt{\frac{\hbar}{eB}}$ where $\hbar$ is Planck's constant divided by 2π. This the spatial extent of an electronic wavefunction in a magnetic field, **B**.

The **electrostatic length**, $l_\varepsilon = \sqrt[3]{\frac{D\hbar}{e\varepsilon}}$, is the spatial extent of an electronic wavefunction in a electric field, ε.

The **Cyclotron radius**, $l_{cycl} = \frac{\hbar k_F}{eB}$, is the radius of a classical cyclotron orbit of a charged particle in a magnetic field, **B**.

Thermal smearing and the associated phase randomisation of an electron of the Fermi distribution produces an energy uncertainty of the order $\mathrm{k}_B\mathrm{T}$. The **thermal length**, $l_T = \sqrt{\frac{D\hbar}{k_B T}}$, determines the dimensionality of electron-electron interactions and is related to the Fermi distribution at temperature T.

The **Bohr radius**, $\mathbf{a_B}$, is the radius of a hydrogen atom in a strongly localised regime and is given by $a_B = \frac{4\pi\varepsilon_o\hbar^2}{e^2 m_o}$, where m_o is the free electron mass and ε_o is the permittivity of free space. The **effective Bohr radius**, $\mathbf{a_B^*}$, is the radial extent of the wavefunction of a hydrogen atom-like donor in a host crystal lattice

having a relative permittivity constant ε_r. The effective Bohr radius is given by $a_B^* = \frac{\varepsilon_r m_o}{m^*} a_B = \frac{4\pi\varepsilon_o\varepsilon_r\hbar^2}{e^2 m_o}$.

The **localisation length**, ξ, is the decay parameter of a wavefunction which is exponentially localised in a disorder potential.

2.2 Density of States (DOS)

The occupied electron states in a 2DEG can be described in terms of their wavevector in the plane, $k_{||}$ and the energy dispersion is:

$$E = E_i + \frac{\hbar^2 k_{||}^2}{2m^*}, \tag{2.3}$$

where E_i is the 2D sub-band energy resulting from confinement in the z direction. Equation 2.3 is valid for parabolic bands, but most cases have a small deviation from parabolicity, usually accounted for as an energy dependence in m^*.

Available electronic states form a lattice of points in k-space with density $\left(\frac{1}{2\pi}\right)^2$ per unit area of sample size. The occupancy of each k-state is limited to $g_s \times g_v$ electrons (due to the Fermionic nature of electrons). The spin degeneracy, g_s, is 2 and the valley degeneracy, g_v, is either 2 for electrons in a Si quantum well or 1 for holes. To minimize the total energy only states within a radius, k_F (Fermi wavevector) of $k = 0$ will be occupied. The Fermi wavevector is:

$$k_F = \sqrt{\frac{4\pi n_s}{g_s g_v}} \tag{2.4}$$

At finite temperatures the surface is blurred over an energy range of $\mathrm{k}_B T$ due to the Fermi-Dirac distribution of occupied states. In typical 2DEGs this is much smaller than $\mathbf{E_F}$.

The rate at which $\mathbf{E_F}$ varies with the sheet carrier density, n_s, is determined by the density of states (DOS) $\mathcal{D}(E)$:

$$\mathcal{D}(E) = \frac{\partial n_s(E)}{\partial E} \tag{2.5}$$

$\mathcal{D}(E)$, is the number of states with energy E per unit area per unit energy and is an important quantity governing several aspects of physical behaviour in the system. The 2D DOS is dependent on energy. At zero temperature all states within the Fermi circle are filled and at finite temperatures the states in a region $\mathrm{k}_B\mathrm{T}$ around $\mathbf{E_F}$ may contribute to conduction. In 2D the states are found, in

k space, within a circle of radius k. The volume of a state is $(2\pi)^2$ and so $\mathcal{D}$ is given by:

$$\mathcal{D}_{2D} = \frac{\partial\left(\pi k^2/(2\pi)^2\right)}{\partial E} = \frac{g_s g_v m^*}{2\pi\hbar^2} \tag{2.6}$$

If more than one 2D sub-band is occupied, each one makes the same contribution to the DOS. Figure 2.1 shows the density of states as a function of energy for a 2D system with only the first 2D sub-band occupied. The shaded region shows the occupied states at a finite temperature.

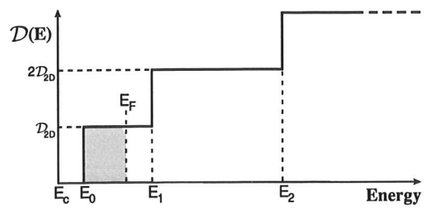

Figure 2.1: The density of states as a function of energy for a 2D system with only the first 2D sub-band occupied. The shaded region shows the occupied states at a finite temperature.

2.3 Transport with No Applied Magnetic Field

It is the ability to control the electrical properties of semiconductors that makes them incredibly useful. The electrical quality of a semiconductor can be determined by simple electrical characterisation techniques, the most important of which are Hall effect measurements. These allow the determination of important parameters such as the mobility and the free carrier concentration.

Under the influence of an electric field, charge carriers in a semiconductor accelerate in a direction parallel to the field. Deviations from the periodic lattice structure due to phonon vibrations and ionised impurities, result in electrons constantly undergoing collisions. These collisions produce scattering events and the overall influence of the electric field on the motion of the charge carriers can be described by the mobility. The mobility is very sensitive to the various scattering mechanisms present in a semiconductor. The average drift velocity v_d of a carrier is proportional to a low electric field $\mathbf{E}$ and the drift mobility μ (the proportionality constant) is given by $v_d = \mu\mathbf{E}$.

A carrier travelling through a semiconductor crystal within $k_B T$ of $\mathbf{E_F}$ can be viewed as a free carrier and so the classical Drude model can be applied. In

the Drude model it is assumed that electrons are randomly scattered by collisions and between these collisions the electrons travel in straight lines. The average time between collisions is given by τ_t, the transport relaxation time. This defines the mean free path as $l = \tau_t v_F$ (as given in Section 2.1.2).

Since all states well below the Fermi surface are occupied, the electrons cannot redistribute among them, so they play no role in charge transport. Therefore a current must be viewed as a redistribution of states close to $\mathbf{E_F}$, which all have roughly the Fermi velocity, $\left(v_F = \frac{\hbar k_F}{m^*}\right)$. This velocity must be large to compensate for the small number of states involved. Typical scattering lengths can on the order of μm and can be larger than lateral device-dimensions achievable by electron-beam lithography.

In the presence of an electric field, $\mathbf{E}$, the current density is:

$$\mathbf{j} = nev = \sigma\mathbf{E} \tag{2.7}$$

This also effectively defines the resistivity, $\rho = \sigma^{-1}$ at $\mathbf{B} = 0$:

$$\mathbf{E} = \rho\mathbf{j} \tag{2.8}$$

The expression for mobility, $\mu = e\tau_t/m^*$ (as given in Section 2.1.2), arises from the equilibrium condition for the average electron velocity in the Drude model, in which electrons are randomly scattered by collisions:

$$m^*\dot{\mathbf{v}} = -e\mathbf{E} - \frac{m^*\mathbf{v}}{\tau_t} = 0 \tag{2.9}$$

This states that an electron is accelerated uniformly in the electric field and then has its momentum randomised, on average after time τ_t (the transport lifetime or momentum-relaxation time), due to some scattering event.

$$\mathbf{v} = -\frac{e\tau_t}{m^*}\mathbf{E} = \mu\ \mathbf{E} \tag{2.10}$$

$$\Longrightarrow \mu = \frac{e\tau_t}{m^*} \tag{2.11}$$

The determination of the mobility at a given temperature can give an indication of the dominant scattering mechanisms that are present. It should be noted that the transport mobility is only limited by scattering events that adversely affect the transmission of current. Thus the transport relaxation time, τ_t, is a measure of the time between large angle scattering events.

Equations 2.7 and 2.11 together give the Drude conductivity relation:

$$\sigma = n_s e\mu = \frac{n_s e^2\tau_t}{m^*} \tag{2.12}$$

2.4 Transport in a Small Magnetic Field

The acceleration of carriers caused by an electric field, **E**, and perpendicular magnetic field, **B** is considered here. In a small **B** field, the transport is complicated by the Lorentz force:

$$m^*\dot{\mathbf{v}} = -e\left(\mathbf{E} + \mathbf{v} \wedge \mathbf{B}\right) \tag{2.13}$$

Since the force on the electrons is no longer parallel to the applied electric field, it is necessary to replace σ and ρ in Equations 2.7 and 2.8 by tensors $\underline{\sigma}$ and $\underline{\rho}$:

$$\begin{pmatrix} j_x \\ j_y \end{pmatrix} = \begin{pmatrix} \sigma_{xx} & -\sigma_{xy} \\ \sigma_{xy} & \sigma_{xx} \end{pmatrix} \begin{pmatrix} E_x \\ E_y \end{pmatrix} \tag{2.14}$$

$$\begin{pmatrix} E_x \\ E_y \end{pmatrix} = \begin{pmatrix} \rho_{xx} & \rho_{xy} \\ -\rho_{xy} & \rho_{xx} \end{pmatrix} \begin{pmatrix} j_x \\ j_y \end{pmatrix} \tag{2.15}$$

Since the motion of electrons in a 2DEG is being considered the above equations can be written as:

$$\begin{pmatrix} j \\ E \end{pmatrix} = \begin{pmatrix} j_x\hat{x} & j_y\hat{y} \\ E_x\hat{x} & E_y\hat{y} \end{pmatrix} \tag{2.16}$$

The force in Equation 2.9 can be replaced by the right hand side of Equation 2.13 to give an expression

$$m^*\frac{d^2r}{dt^2} = -\frac{m}{\tau_t}\frac{dr}{dt} - eE - e\left(\frac{dr}{dt} \times B_\perp\right) \tag{2.17}$$

By considering the steady state solution this can be solved to give

$$v_x = -\mu E_x - \frac{e\mathbf{B}}{m^*}\tau_t v_x \tag{2.18}$$

$$v_y = -\mu E_y - \frac{e\mathbf{B}}{m^*}\tau_t v_y \tag{2.19}$$

$$v_z = -\mu E_z \tag{2.20}$$

The term $e\mathbf{B}/m^*$ is referred to as the cyclotron frequency ω_c and describes the frequency of the electron orbit around the magnetic field lines. In the absence of scattering electrons at $\mathbf{E_F}$ undergo an orbital motion at the cyclotron frequency, ω_c and with the cyclotron radius, l_{cycl}. For small magnetic fields, however, scattering prevents the electrons from performing complete orbits so when $\omega_c\tau_t << 1$, the magnetic field only causes a transverse perturbation to the electric field.

The classical model does not predict any variation of the resistance with temperature or magnetic field even if there is a constant scattering rate. The values of the transport coefficients can be calculated with equation 2.17. Since carriers are confined in the x-y plane, the perpendicular component of the electric field, $E_\perp$ is also equal to zero and so:

$$\underline{\sigma} = \frac{\sigma_o}{1+(\omega_c\tau_t)^2}\begin{pmatrix} 1 & -\omega_c\tau_t \\ \omega_c\tau_t & 1 \end{pmatrix} \tag{2.21}$$

$$\underline{\rho} = \rho_o\begin{pmatrix} 1 & \omega_c\tau_t \\ -\omega_c\tau_t & 1 \end{pmatrix}, \tag{2.22}$$

For a Hall bar geometry, $j_y = 0$, and measurements with such a device yield ρ_{xx} and ρ_{xy} directly, while the components of $\underline{\sigma}$ must be calculated by inverting $\underline{\rho}$:

$$\sigma_{xi} = \frac{\rho_{xi}}{\rho_{xx}^2 + \rho_{xy}^2} \qquad i = x, y \tag{2.23}$$

The 2DEG is confined to a Hall bar thus preventing any current from flowing in the y direction and so:

$$\rho_{xx} = \frac{E_x}{J_x} = \frac{1}{ne\mu} \tag{2.24}$$

$$\rho_{xy} = \frac{E_y}{J_x} = -\frac{\mathbf{B}}{ne} \tag{2.25}$$

In the longitudinal direction this gives the standard equation for motion in an electric field. However due to the effect of the magnetic field a voltage is built up across the Hall bar. This is known as the Hall voltage and can be used to calculate the carrier density, n_s. The classical Hall effect is given by $\rho_{xy} = R_H\mathbf{B} = \mathbf{B}/en_s$ which is used to determine n_s (R_H is the Hall coefficient). Since the Hall voltage is dependent on the charge of the carrier, it can be used to differentiate between electron and hole transport.

2.4.1 Small-Field Transport Corrections

It is also possible to describe transport in terms of electron diffusion. By considering both the particle flux and the electrochemical potential ($\tilde{\mu}$) in equilibrium ($\nabla\tilde{\mu} = 0$), one can derive the Einstein relation:

$$\sigma = \mathcal{D}(E_F)e^2D \tag{2.26}$$

This equation shows that the classical conductivity is modified if there is any change in either the diffusion constant (affected by localisation) or the DOS at the

$\mathbf{E_F}$ (affected by electron-electron interactions). These leads to correction terms in the low-field conductivity.

Weak Localisation

When an electron travels diffusively from one point A to another B, within its phase-coherence time, τ_ϕ, the wavefunction (amplitude $\mathcal{A}$) for any path interferes with wavefunctions travelling along all other possible paths. Generally the waves are out of phase with each other and since all of the paths differ, the average probability of the electron travelling from A to B by any given path is $|\mathcal{A}|^2$. For any paths from A to B which pass through the start-point A again, there is a corresponding path which is the exact reverse. The amplitudes $\mathcal{A}_+$ and $\mathcal{A}_-$ for the two paths are in-phase and interfere constructively to give a back-scattering probability of $|2\mathcal{A}|^2/2 = 2|\mathcal{A}|^2$ per path. The probability of the electron returning to its start-point is enhanced, leading to localisation.

The effects of localisation are derived from scaling theory [63, 64]. This considers variation of conductance in a system size, L, in terms of a scaling function, $\mathcal{B}(g) = \frac{\partial(\ln g)}{\partial(\ln L)}$ in which g is a dimensionless conductance (in units of e^2/h). In ideal systems with dimension d, the scaling function is $\mathcal{B}(g) = (d-2)$, but for weak disorder ($k_F l >> 1$), coherent back-scattering reduces this to:

$$\mathcal{B}(g) = (d-2) - \pi^{-2}/g, \tag{2.27}$$

(π^{-2} applies to a gas of fermions) [65].

In non-interacting 2D systems, Equation 2.27 implies that all states are localised at T = 0 K [64]. Integrating equation 2.27 for 2D leads to an expression for the conductivity correction:

$$\Delta\sigma_{loc}(L) = -\frac{\tilde{\alpha}e^2}{\pi^2\hbar}\ln\left(\frac{L}{L_o}\right) \tag{2.28}$$

where $\tilde{\alpha}$ is a constant whose value depends on the different scattering mechanisms [66, 67].

The effect of magnetic flux threading along a closed path introduces a phase difference, $\Delta\phi = \frac{2e}{\hbar}\oint \mathbf{A}.d\mathbf{x}$, between time-reversed paths $\mathcal{A}_+$ and $\mathcal{A}_-$. Each pair of paths will have a slightly different phase and so enhanced backscattering may be lost. When there is no magnetic or spin-orbit scattering, this leads to a

conductivity correction of:

$$\delta\sigma_{loc}(T,\mathbf{B}) = \frac{\tilde{\alpha}e^2}{2\pi^2\hbar}\left[\psi\left(\frac{1}{2}+\frac{\hbar}{4e\mathbf{B}\mathcal{D}\tau_\phi}\right) - \psi\left(\frac{1}{2}+\frac{\hbar}{4e\mathbf{B}\mathcal{D}\tau_{el}}\right) + \ln\left(\frac{\tau_\phi}{\tau_{el}}\right)\right], \tag{2.29}$$

see [66, 68] for more details.

At T = 0 K with no applied field the system size should be the size of the sample. This gives a T-dependent conductivity correction:

$$\Delta\sigma_{loc}(T) = -\frac{\tilde{\alpha}pe^2}{2\pi^2\hbar}\ln\left(\frac{T}{T_o}\right) \tag{2.30}$$

p is the temperature exponent of the inelastic scattering time, $\tau_{in} \sim T^{-p}$, which depends on the dimensionality and scattering mechanisms.

Equation 2.29 gives the expected boundary conditions for $\Delta\sigma_{loc}(T,\mathbf{B})$. At zero field $\Delta\sigma_{loc}(T,\mathbf{B}) \rightarrow \mathbf{0}$ and at high fields it approaches $\Delta\sigma_{loc}(T,\mathbf{B}) \rightarrow -\mathbf{\Delta\sigma_{loc}(T)}$, thereby removing the localisation correction.

Electron-Electron Interactions

Introducing electron-electron interactions into an electron system gives rise to a dip in the DOS at the $\mathbf{E_F}$. This effect is reduced by screening, which results in a logarithmic temperature dependence [68, 69]. This logarithmic dependence is the same as for weak localisation making it almost impossible to isolate the two effects with T-dependent conductivity measurements. A magnetic-field dependence in electron-electron interaction effects [70, 71] resulting from spin-splitting means that electron-electron effects are not sensitive to the field direction for most systems unlike weak localisation which requires a perpendicular magnetic field. Corrections resulting from electron-electron interactions are given by:

$$\Delta\sigma_{int}(T,\mathbf{B}) = \frac{e^2}{2\pi^2\hbar}\left(1-\frac{3}{4}\tilde{F}_\sigma\right)\ln\left(\frac{T}{T_0}\right) - \frac{e^2}{2\pi^2\hbar}\frac{\tilde{F}_\sigma}{2}g_{2D}(\omega) \tag{2.31}$$

where $\omega = g\mu_B B/k_B T$ and $g_{2D}(\omega)$ is a function [71] where:

$$g_{2D}(\omega) = \begin{cases} \ln(\omega/1.3), & \omega >> 1 \\ 0.084\omega^2, & \omega << 1 \end{cases} \tag{2.32}$$

The temperature dependence of the Hall coefficient in the presence of weak localisation and electron-electron interactions has been considered by Altshuler *et al.* [68]. It was shown that whilst localisation has no effect on R_H, electron-electron interactions give a correction of $\frac{\Delta R_H}{R_H} = 2\frac{\Delta\rho}{\rho}$ where $\Delta\rho$ is the T-dependent

correction of equation 2.31. This gives:

$$\Delta R_H = -R_H \rho \frac{e^2}{\pi^2 \hbar} \left(1 - \frac{3}{4}\tilde{F}_\sigma\right) \ln\left(\frac{T}{T_o}\right), \tag{2.33}$$

which provides a method for distinguishing between the two logarithmic conductivity corrections. More details on weak localisation and electron-electron interactions can be found in [65].

2.5 Transport in a Quantising Magnetic Field

2.5.1 Landau Levels (LLs)

The energy eigenstates for a three-dimensional (3D), free electron gas can be found from the solution of the time-independent Schrödinger equation,

$$\frac{-\hbar^2}{2m}\nabla^2\psi + V\psi = E\psi \tag{2.34}$$

with ψ given by the Bloch function $Ae^{(ikr)}$, and k is the wavevector.

When a strong magnetic field is applied ($\omega_c \tau_q > 1$), the classical formalism can no longer be applied because the field causes the electron system to form a new set of eigenstates. These are derived by replacing the momentum, $\mathbf{p}$ in the Hamiltonian, by $\mathbf{p} - q\mathbf{A}$, where q is the charge and $\mathbf{A}$ is the vector potential (such that $\nabla.\mathbf{A} = 0$ and $\nabla \wedge \mathbf{A} = \mathbf{B} =< 0, 0, B_\perp >$). Even if the magnetic field has a component in the plane it will have no effect on the energy level structure [72].

The energy of a carrier in a magnetic field can be shown to be quantised, by solving the Schrödinger equation.

The Hamiltonian can be written as:

$$H = \frac{p_x^2}{2m^*} + \frac{m^*\omega_c^2}{2}(x - x_o) \tag{2.35}$$

where p_x is the momentum operator.

In 2D, when the electron motion is constrained to a plane that is orthogonal to the applied magnetic field, $B_\perp$, the Schrödinger equation is modified and the 2DEG energy levels for single sub-band occupancy are split and replaced by a set of well defined energy levels, given by:

$$E_n = \left(n_L + \frac{1}{2}\right)\hbar\omega_c + \frac{\hbar^2 {k_z}^2}{2m^*} \tag{2.36}$$

$$E_n = E_z + \left(n_L + \frac{1}{2}\right)\hbar\omega_c \qquad n_L = 0, 1, 2, \ldots \tag{2.37}$$

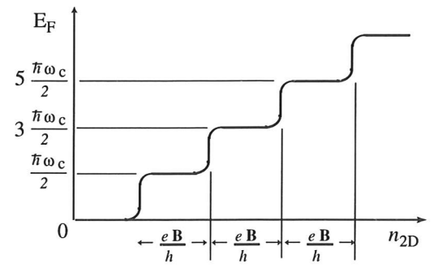

Figure 2.2: $\mathbf{E_F}$ in a 2D system as a function of carrier density, n_{2D} at fixed magnetic field, B.

n_L is a positive integer known as the Landau index, k_z is the wavevector in the direction parallel to the magnetic field and E_z is energy of the lowest 2D sub-band. Equation 2.37 shows that the eigenvalues of a 2D system lie on integer multiples of $\hbar\omega_c/2$. Each of these discrete states is known as a Landau level (LL). The $\mathbf{E_F}$ in a 2D system as a function of carrier density, n_{2D} at fixed magnetic field, $\mathbf{B}$, is shown in Figure 2.2.

Since the total number of electrons is unchanged, in a strong field the LLs become highly degenerate (the degeneracy corresponding to one per flux quantum threading the sample: $eB_\perp/h$ per unit area).

If the electron spin is included in Equation 2.34 then the eigenvalues take on the form:

$$\varepsilon_n = E_n + (l + \frac{1}{2})\hbar\omega_c + m_s g \mu_B \mathbf{B} \tag{2.38}$$

E_n is the energy due to z confinement, l is an integer, m_s is the spin quantisation number ($m_s = \pm\frac{1}{2}$), g is the *Landé* g-factor and μ_B is the Bohr magnetron, $\mu_B = \frac{e\hbar}{2m^*}$

When using Si based material, the valley splitting in Si further splits each spin-split state into 2, as shown in Figure 2.3.

Density of States in a Landau Level

In the absence of a magnetic field, the density of states (DOS) of a 2DEG is constant as given in Equation 2.6. In a perpendicular magnetic field, $B_\perp$, the DOS becomes a set of discrete δ-functions with an energy separation of $\hbar\omega_c$.

In the presence of spin and valley degeneracy, the Fermionic electrons avoid occupying the same states by becoming spatially localised. The important length scale for these states is the magnetic length, l_B.

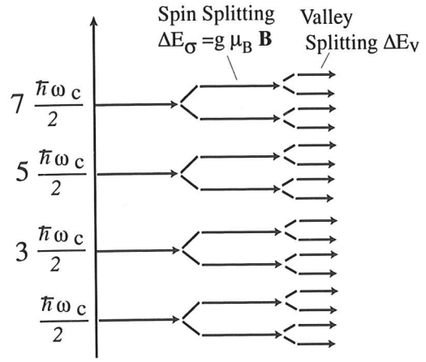

Figure 2.3: The spectrum of a 2D system in a strong B field showing basic Landau levels, spin split and valley split levels from left to right.

As the field is increased, the degeneracy increases, so that for a fixed carrier density, the number of occupied LLs falls. The filling factor, ν, is defined as the ratio of the electron density to the number of states per LL (when spin splitting is resolved) and hence is equal to the number of Landau levels filled:

$$\nu = \frac{h}{e\mathbf{B}} n_{2D} \tag{2.39}$$

Generally the total number of carriers n_{2D} is fixed. As the **B** field increases the number of states that can be accommodated in each LL also increases. A slight increase in **B** field allows more states to be contained in each LL. At a critical field the electrons can all be accommodated in the lower LLs and so the $\mathbf{E_F}$ drops into the lower LL. Therefore as the magnetic field is increased the number of states that can be contained per LL increases and so the Fermi surface oscillates. In reality, $\mathbf{E_F}$ varies very smoothly due to the finite width of the levels, and to the presence of gap states. A Landau-level fan of states at $(\mathrm{N} + \frac{1}{2})\hbar\omega_c$ as a function of **B** for each n in Figure 2.4. The bold line shows the oscillatory behaviour of $\mathbf{E_F}$ as a function of magnetic field at constant carrier density. The zero field value is shown by the broken line.

2.5.2 Landau Level Broadening

Although the LL are ideally δ functions, in a real system at finite temperatures the sharp LLs are broadened in a number of ways. There is an energy broadening, k_BT at finite temperatures, disorder from impurities and lattice vibrations and

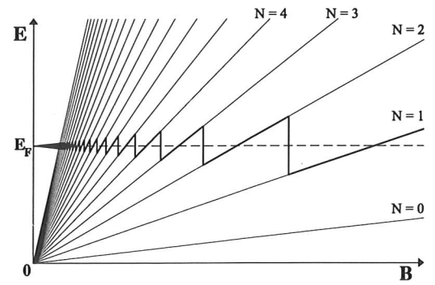

Figure 2.4: A LL fan of states at $(\mathrm{N} + \frac{1}{2})\hbar\omega_c$ as a function of **B** for each n. The bold line shows the oscillatory behaviour of $\mathbf{E_F}$ as a function of magnetic field at constant carrier density. The zero field value is shown by the broken line.

from other sources of scattering. Scattering causes broadening due to the time-energy uncertainty relation and the resultant band profile is [61, 73]:

$$\mathcal{D}(E) = \frac{1}{2\pi l_B^2}\frac{2}{\pi\Gamma_N}\sum_N \left[1 - \left(\frac{E - E_N}{\Gamma_N}\right)^2\right]^{\frac{1}{2}}, \tag{2.40}$$

where Γ is independent of N when $\tau_t = \tau_q$ and is given by:

$$\Gamma^2 = \frac{2}{\pi}\hbar\omega_c\frac{\hbar}{\tau_t} \tag{2.41}$$

A large proportion of the states of the DOS in a **B** field, are localised and exist between the LLs. The proportion of states which are localised depends on the strength of the disorder in the sample. The DOS is broadened by potential fluctuations in the system which cause the energy of each LL to vary with position. Near the edges of a disorder-broadened LL, states are localised over a short distance by the potential profile and this localisation length increases exponentially as the centre of the band is approached.

2.5.3 Degenerate Landau Level Splittings

The degeneracy of the momentum states mentioned in section 2.2 means that the description of energy levels in a quantising magnetic field is slightly more complicated for Si/SiGe heterostructures. The energy of electrons in different spin and different valley-states also has a magnetic-field dependence.

When a large field is applied, the degeneracies are lifted and the regular ladder of LLs is further broken up into non-degenerate levels, usually with irregular spacings. When the degeneracies are lifted, the definition of ν in equation 2.39

remains unaltered, with ν being the number of *non-degenerate* levels occupied. Therefore, the lowest LL ($N = 0$) is full when $\nu = g_s g_v$.

In the case of the valley splitting, a small splitting is believed to exist at zero-field [61]. The origin of this effect is not well understood, though a number of models have been proposed to explain it, as discussed in Ref. [61]. Mechanisms have included spin-orbit coupling, k-space tunnelling [74], surface scattering [75] and it has been suggested that in Si/SiGe systems, alloy disorder may play a role [76].

The spin splitting originates from the Zeeman effect, which gives the electrons an additional energy, $m_s g \mu_B \mathbf{B}$ where the quantum number of spin resolved along the field direction, $m_s = \pm\frac{1}{2}$, hence giving a splitting of $\Delta E_s = g\mu_B \mathbf{B}$. The size of the splitting is dependent on g, the *Landé* g-factor. This is 2 for a free electron but in 2D systems different values of g have been measured [72] and this has been explained as a consequence of the exchange interaction.

From the Pauli exclusion principle no two particles can occupy a state and so there is a reduced probability of finding two electrons with the same spin state close to each other. Coulomb repulsion will enhance the energy of two closely-spaced electrons and so the exchange interaction leads to an energy reduction proportional to the number of electrons in the same spin state.

When the Fermi level is between spin-split levels, the interactions with lower levels are equal for spin-up and for spin-down. The lower spin-up level contains more electrons and so an electron with spin-up will be reduced in energy more than the electrons with spin-down, leading to an additional splitting proportional to $(n_\uparrow - n_\downarrow)$. There is expected to be an oscillation in the g enhancement as the relative population of different spin levels changes (with $\mathbf{B}$ or with n_s [77]). If the LLs overlap significantly (occurs with low $\mathbf{B}$ fields), the enhancement cannot reach its minimum value, and the effective g tends to a constant, enhanced value [77, 78]. For well-separated levels, g should be recovered when the spin populations are equal. Evidence has been presented for an exchange enhancement of the gap between different LLs [79], which gives an apparent reduction of g.

2.5.4 Shubnikov-de Haas (SdH) Oscillations

The LLs are composed of areas of extended states (in the centre of the LL) which are free to transport charge in the presence of an electric field. Current flow is possible only through these extended states. The localised states present in

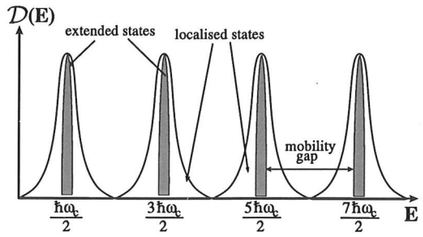

Figure 2.5: Landau levels in the presence of disorder. The density of states is shown as a function of energy in a magnetic field, illustrating the band of lifetime-broadened extended states and disorder-induced localised states in the gap.

the tails are caused by disorder. Figure 2.5 shows the DOS in a magnetic field, showing that a large number of states are localised and exist between the LLs.

At intermediate $\mathbf{B}$ fields, LLs are beginning to form but are not clearly separated in energy. It is possible to treat the system as having an oscillatory perturbation in the DOS [80]. Isihara and Smrčka [81], have calculated this oscillation to be:

$$\frac{\Delta\mathcal{D}}{\mathcal{D}_0} = 2\sum_{s=1}^{\infty} \exp\left(\frac{-\pi s}{\omega_c \tau_q}\right) \frac{s\chi}{\sinh(s\chi)} \cos\left(\frac{2\pi s E_F}{\hbar\omega_c} - \pi s\right), \tag{2.42}$$

$$\chi = 2\pi^2 k_B T/\hbar\omega_c \tag{2.43}$$

The cosine term describes the oscillation while the exponential term gives the magnetic-field damping which results from the increasing overlap of the LLs as the splitting gets smaller at lower fields. The other term in the summation is a thermal damping factor (to account for the thermal smearing of the energy levels at non-zero temperatures). At very low temperatures, this factor reduces to 1, since thermal smearing is small compared to scattering.

Conductivity is governed by the states at the Fermi surface and so can be related to the DOS. The oscillations in conductivity can be related to equation 2.42 by generalising equation 2.21 as follows [81, 82]:

$$\sigma_{xx} = \frac{e^2}{m^*} \frac{\tilde{\tau}_t}{(1 + \omega_c^2 \tilde{\tau}_t^2)} \tilde{n}_s(E_F), \tag{2.44}$$

$\tilde{n}_s(E_F) = n_s\left(1 + \frac{\Delta\mathcal{D}}{\mathcal{D}_0}\right)$ and $\tilde{\tau}_t = \tau_t(\mathcal{D}_0/\mathcal{D})$. A similar expression is given for the transverse conductivity:

$$\sigma_{xy} = -\omega_c \tilde{\tau}_t \sigma_{xx} + e\frac{\partial N(E_F)}{\partial B}, \tag{2.45}$$

$N(E_F)$ is the number of states below the Fermi level. The first term is from equation 2.21, while the second term accounts for the quantisation of σ_{xy} at high fields [83]. This term can be simplified by using the approximations $\hbar/2\tau_q \ll E_F$, $\hbar\omega_c/2\pi s \ll E_F$ and $\Delta\mathcal{D}/\mathcal{D}_0 \ll 1$. These equations can be inverted to give simple expressions for the resistivity:

$$\rho_{xx} = \frac{1}{\sigma_o}\left[1+2\frac{\Delta\mathcal{D}(E_F)}{\mathcal{D}_0}\right] \tag{2.46}$$

$$\rho_{xy} = \frac{\omega_c\tau_t}{\sigma_o}\left[1-\frac{1}{\omega_c^2\tau_t^2}\frac{\Delta\mathcal{D}(E_F)}{\mathcal{D}_0}\right] \tag{2.47}$$

The first of these describes magnetoresistance oscillations that are more commonly known as Shubnikov de Haas (SdH) oscillations.

Taking just the first term in the summation of equation 2.42, the amplitude of the oscillation of these quantities is given by:

$$\Delta\rho_{xx} = -2\omega_c\tau_t\Delta\rho_{xy} = 4\rho_o\frac{\chi}{\sinh(\chi)}\exp\left(\frac{-\pi}{\omega_c\tau_q}\right) \tag{2.48}$$

This can be used to derive the quantum lifetime, τ_q. A plot of $\log(\Delta\rho_{xx})$ vs. $1/\mathbf{B}$ (known as a Dingle plot) will have a slope of $-\frac{\pi m^*}{e\tau_q}$. In principle, the same can be done for ρ_{xy}, but these oscillations are generally much smaller which makes this more difficult.

The extent to which the LL are filled will affect the longitudinal electrical properties. If the $\mathbf{E_F}$ of the 2DEG lies within the extended states it behaves like a metal with a partially filled band, leading to conductivity. However if $\mathbf{E_F}$ lies within the localised states the bands are completely full below $\mathbf{E_F}$ and empty above leading to insulator-like behaviour. The conductance will reach a maximum when the bands are half filled $n = \left(l+\frac{1}{2}\right)\frac{2e\mathbf{B}}{h}$ and are a minima when $n = l\frac{2e\mathbf{B}}{h}$. The separation in $\mathbf{B}$ field between adjacent LLs (peaks in the SdH oscillations), can be used to determine the carrier concentration of the 2DEG, from:

$$n_{2deg} = \frac{g_s g_v e}{h}\frac{1}{\Delta(1/\mathbf{B})} \tag{2.49}$$

By inverting the conductivity tensor, it can be experimentally shown that as the conductivity drops to zero, so does the resistivity. In terms of the conductivity σ, the experimentally measured quantity, ρ_{xx} is given by:

$$\rho_{xx} = \frac{\sigma_{xx}}{\sigma_{xx}^2+\sigma_{xy}^2} \tag{2.50}$$

The resistivity therefore will oscillate similarly to the conductivity and can changes as the applied magnetic field is varied. This is a result of the localised states in between LLs which cannot carry current. When $\mathbf{E_F}$ lies in this region, the filling factor is an integer and any scattering events cannot provided enough energy to scatter an electron to a higher, unoccupied LL (all the lower ones being occupied), thus the resistivity is zero. There is an accurate quantisation of the Hall conductance at $\sigma_{xy} = \nu e^2/h$ and the simultaneous vanishing of σ_{xx} (ρ_{xy} and ρ_{xx} are then equal to $h/(\nu e^2)$ and zero respectively).

2.5.5 The Quantum Hall Effect (QHE) Regime

Two conditions have to be met for the effect of the magnetic field to be observed; the thermal broadening has to be less than the separation between the levels - $kT \ll \hbar\omega_c$ and the mean scattering time τ_t, has to be large such that the electron can complete a few cyclotron orbits before being scattered, *i.e.* $\omega_c\tau_t > 1$.

To satisfy these requirements, measurements have to be made at low temperatures with very pure samples. It has been shown that LL spacing is proportional to the magnetic field. As the magnetic field is swept, the DOS at the $\mathbf{E_F}$ oscillates. There are maxima when $\mathbf{E_F}$ is in the centre of a LL, and minima when $\mathbf{E_F}$ is in between LLs. In a strong magnetic field, the extended states of the LLs become well separated in energy and it is in this regime that it is possible to observe the well-known Quantum Hall effect (QHE). This was first demonstrated in 1980 [84] for a 2DEG in a Si MOS inversion layer and has since been extensively studied in a variety of systems.

The transverse conductivity and resistivity remain finite by current flowing through the extended states. Integrating equation 2.6 gives the number of states per unit area, and by substituting in Equation 2.37, this leads to:

$$\Delta n = \frac{2eB_\perp}{h} \tag{2.51}$$

Therefore, the total number of states per unit area at the $\mathbf{E_F}$, assuming ν LLs below E_f are filled is

$$N_{tot} = \frac{2e\nu B_\perp}{h} \tag{2.52}$$

The Hall resistivity can now be written in terms of N_{tot}, such that:

$$\rho_{xy} = \frac{h}{2\nu e^2} \tag{2.53}$$

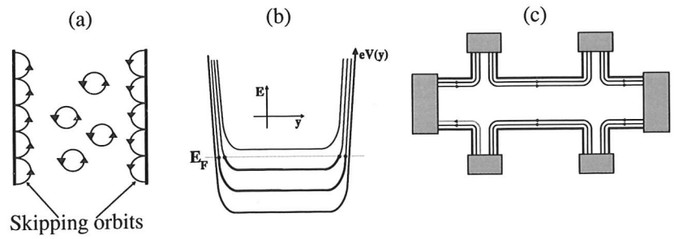

Figure 2.6: (a) The skipping orbits along the edge of a device. (b) The electrostatic potential near the barrier are raised and so the LL rise in energy as they approach the edge and forming edge states. (c) Transport in the QHE regime via edge channels for a Hall bar geometry.

Due to the imperfections in a real crystal and the existence of localised states, the Hall resistivity and conductivity are constant and exhibit plateaux which take the value of integer multiples of $\frac{2e^2}{h}$, independent of the material systems the measurements are done on. This phenomenon is referred to as the Quantum Hall Effect. The accuracy of the values of the Hall resistivity plateaux have been found to be better than 1 part in 10^7 and the above equation is now used as the universal resistance standard.

Classically the electrons are considered to be traveling in cyclotron orbits. The quantum mechanical picture is more complex and requires consideration of edge states. If an electron is too close to the edge of a device, a full orbit cannot be completed and transport occurs due to skipping orbits (shown in figure 2.6a). At the sample edges the confining potential causes the levels to bend up and cross $\mathbf{E_F}$ (shown in figure 2.6b). The group velocity is defined as:

$$v_g = \frac{1}{\hbar}\frac{\partial E(k)}{\partial k} = \frac{1}{\hbar}\frac{\partial E}{\partial y_o}\frac{\partial y_o}{\partial k}, \tag{2.54}$$

Electrons in localised states in the bulk region do not move ($\frac{\partial E}{\partial y_o} = 0$), as only delocalised states can carry current across the sample. Electrons at the edge travel along in opposite directions at either side of the sample, corresponding to classical skipping orbits (shown in figure 2.6a) and net transport in the QHE is governed by these edge states (shown in Figure 2.6c). The edge channels are expected to be very narrow, though in reality, solving the electrostatics self-consistently shows that the LL becomes pinned at $\mathbf{E_F}$, forming a conducting strip [85]. Nonetheless, since the strip contains electrons in states from a single magnetic sub-band, the transport within them is 1D in nature.

As the magnetic field increases, a LL immediately below $\mathbf{E_F}$ will move up to

meet it and at this point the edge state moves towards the central bulk region and becomes depopulated. Buttiker used an edge state model to give an explanation of the resistance observed in the QHE [86]. Details of this theory are above the scope of this thesis (a brief description is provide in Section 2.6), but it shows that the conductance of an edge state is quantised. As the edge state depopulates the resistance increases by $\frac{h}{e^2}$ and $\mathbf{E_F}$ is in the gap between LL and so no further increase in resistance is seen, forming a plateau, until the next edge state depopulates.

2.6 The Landauer Buttiker Formalism (LBf)

The LBf [86] is a treatment of multi-probe transport measurements of a system of 1D conducting channels, in which the role of the contacts is emphasised. Contacts are assumed to be ideal with no resistance. Incoming states are transmitted into the contact without reflection, and outgoing states are in equilibrium at an electrochemical potential, $\tilde{\mu}$, equal to that of the contact. Non-ideal behaviour of the contacts can be accounted for in terms of reflection coefficients of the channels.

The transport properties of a 1D system depend on the DOS, which is:

$$\mathcal{D}_{1D} = \frac{\partial n}{\partial k}\frac{\partial k}{\partial E} = \frac{g_s g_v}{2\pi}\frac{\partial k}{\partial E} \tag{2.55}$$

for forward-travelling modes (n is the number of occupied states). This can then be combined with the group velocity to give:

$$I = -ev_g\mathcal{D}\Delta\tilde{\mu} = -g_s g_v\frac{e}{h}\Delta\dot{\mu} \tag{2.56}$$

This expression shows that the DOS and the group velocity cancel out in 1D, to give a current that is only dependent on changes in electrochemical potential. Hence for a system of 1D channels, there is a quantised conductance:

$$G = Mg_s g_v\frac{e^2}{h} \tag{2.57}$$

where M is the number of occupied channels. This has been observed in narrow constrictions in high quality 2D systems [87, 88], but the generality of equation 2.56 means that it can be applied also to edge states in a magnetic field [86].

A general treatment of transport in these systems requires the possibility of scattering between different channels, characterised by the reflection coefficients,

$\mathcal{R}_i$ (the probability of an electron from contact i being back-scattered to the same contact) and transmissions coefficients, $\mathcal{T}_{ji}$ (the probability of an electron from contact i being transmitted to contact j). These coefficients need to be summed over paths involving all possible combinations of 1D channels. The net current coming out of contact i is then given by:

$$I_i = -\frac{e}{h}\left(\left(M - \sum_{channels} \mathcal{R}_i\right)\tilde{\mu}_i - \sum_{channels}\sum_{j\neq i} \mathcal{T}_{ji}\tilde{\mu}_j\right) \tag{2.58}$$

In the case of the QHE, localisation of the channels at opposite sides of the sample means that back-scattering is greatly suppressed and current from a contact transmits perfectly into the next contact. This is unaffected by any scattering between adjacent edge modes and so the filling factor, ν, is the number of non-degenerate channels. When $\mathbf{E_F}$ lies in the extended states in the bulk of the sample, back-scattering readily occurs, but only for the inner-most channel. This mode makes only a partial contribution to the transport, and ρ_{xy} takes a value between the quantised plateaux. Back-scattering also leads to a potential drop along the sample, giving a non-zero ρ_{xx}.

2.7 Scattering Mechanisms

2.7.1 Scattering Lifetimes

An electron travelling through a semiconductor is subjected to several mechanisms that cause it to deflect, or scatter, from its original path. If this deflection is through a large angle then it will reduce the momentum relaxation time, τ_t, which reduces the transport mobility. A small angle deflection will not affect the transport mobility significantly but is reflected in the quantum lifetime τ_q.

The transport lifetime, τ_t, is the time between collisions which relax the momentum and so have an isotropic angular scattering distribution, $P(\theta)$. However in high-mobility modulation-doped structures, the mobility can be limited by scattering from the remote ionised impurities in the doping layer. The disorder potential arising from these is long-range in nature and so there is a predominance of small angle scattering and τ_t is weighted by direction:

$$\frac{1}{\tau_t} = \int P(\theta)(1-\cos\theta)\, d\Omega \tag{2.59}$$

θ is the scattering angle and $P(\theta)$ is the scattering cross section.

The quantum lifetime τ_q is the lifetime of an electron in a particular momentum state and this governs the degree of energy-level broadening as a result of the time-energy uncertainty relation.The true scattering time τ_q, is :

$$\frac{1}{\tau_q} = \int P(\theta)\, d\Omega \tag{2.60}$$

This does not contain a directional term $(1-\cos\theta)$ and so all scattering events are included. The different scattering times, τ_x, combine to give a total scattering time $\frac{1}{\tau} = \sum_x \left(\frac{1}{\tau_x}\right)$, so the overall scattering rate is limited by the shortest scattering time. The transport lifetime τ_t will be larger than the quantum lifetime, τ_q, as pointed out by Coleridge *et al.* [82].

The ratio of the two scattering times, $\alpha = \tau_t/\tau_q$, can give information on the type of scattering occurring in the sample. If α is close to 1 it implies that the scattering is predominantly large angle which is the case for short-range impurity potentials. If there are more large range scattering events, such as from modulation doping, then τ_q would be expected to be much less than τ_t, giving a large value for α.

There are a number of other scattering mechanisms which may affect the mobility. These may be divided into elastic processes (these preserve the energy of the state) and inelastic processes (these alter the energy of the state). At high temperatures, the dominant mechanism is usually phonon scattering (an inelastic process), but at low temperatures the mobility in a semiconductor is normally limited by one of the elastic scattering mechanisms.

2.7.2 Inelastic Scattering Mechanisms

Electron-phonon and electron-electron scattering are the two main inelastic scattering mechanisms. At low temperatures very few phonons can be excited and so this is not normally a dominant mechanism. Inelastic mechanisms destroy the phase coherence of the electron wavefunction, so they also determine the phase-relaxation time, τ_ϕ.

Phonon Scattering

At high temperatures optical and acoustic phonons cause a large amount of scattering. This effect is reduced with temperature, with scattering due to optical phonons reduced considerably by 50 K. Acoustic phonons scattering dominate be-

low 50 K but their contribution decreases with falling temperature and at liquid He temperatures they may be neglected (this depends on the 2DEG quality).

Deformation Potential

This is an acoustic phonon mode of scattering and is caused by lattice vibrations deforming the equidistant spacing between the lattice constituents. The bandgap varies from point to point, thus producing a scattering potential. The mobility limit in this scattering regime was first calculated by Bardeen and Shockley [89].

Electron-electron scattering

Electron-electron scattering is strongly affected by temperature, since both electrons have to scatter into unoccupied states close to the Fermi surface in order to conserve the total energy. Electron-electron interactions are stronger for higher electron densities, so this scattering rate is expected to be proportional to $\mathbf{E_F}/\mathrm{T}^2$.

2.7.3 Elastic Scattering Mechanisms

Elastic mechanisms include scattering from impurity potentials, such dopants which have deliberately added or from unintentional background impurities. Disorder potentials from interface-roughness, alloy scattering and from lattice defects and dislocations, may give rise to further elastic scattering. Since the energy of the state is not changed in elastic scattering processes, the phase coherence of the wavefunction is preserved.

Interface Roughness Scattering

Interface roughness scattering is caused by disorder present at the Si/SiGe interface. The roughness is a complicated function of the growth conditions. In general the maximum mobility limit placed by interface roughness is higher than the limits of background impurity or from remote ionised impurity scattering and in the highest quality wafers the effects of interface roughness scattering can become significant as contributions from other scattering mechanisms become small.

Ionised Dopant Impurity Centres in the SiGe layer

Scattering of electrons by the Coulomb potential is an important problem. This scattering mechanism involves elastic scattering of carriers from the ionised centres that are introduced into a pure semiconductor. The Brookes-Herring formula [90] adequately describes the mobility versus temperature relationship of this mechanism when it dominates at low temperatures. The Coulomb potential is exponentially reduced by the presence of an undoped SiGe layer between the doped region and the interface. This spacer layer reduces the number of carriers able to reach the channel and so there is a balance between the width of the spacer and the carrier density, n_s. This also implies that there is a maximum mobility that can be achieved for a particular depth of the 2DEG.

Ionised Impurity Centres in the conducting channel

These are present due to residual impurities in the growth chamber. The density of these impurities varies depending on the growth technique used and the cleanliness of the growth chamber used.

Theoretical scattering potential curves have been calculated using Boltzmann approximations, which show that phonon scattering dominates at high temperatures while ionised impurity scattering is the limiting factor at low temperatures. In real samples with both intentional and unintentional impurities, the mobility is seen to peak at temperatures that depend on the total impurity concentration of the material.

Chapter Summary

This chapter summarised the principles of transport in two dimensional gases as well as providing a brief description of the various length scales referred to throughout this thesis, in Section 2.1.

The main focus has been on 2DEGs, but with an appropriate change of sign and effective mass, the analysis presented here applies equally well to 2DHGs. Section 2.3 describes the transport properties of and two dimensional gas when there is no applied magnetic field. The effects of an applied magnetic field are covered in Sections 2.4 and 2.5 and there is an introduction to one dimensional transport that has been included in Section 2.6.

A summary of different scattering mechanisms and scattering lifetimes has

been included at the end of this chapter in Section 2.7. This section includes a definition of the different scattering lifetimes that are referred to throughout this thesis as well as a description of some of the elastic and inelastic scattering processes that can have an effect on device performance.

Chapter 3

Si/SiGe Wafer Growth and Device Fabrication

Introduction

The ability to fabricate a heterojunction at moderate temperatures (between 400°C to 700°C) permits the growth of SiGe layers on Si wafers already possessing the proper chemical regions for electronic devices, without distorting the pre-existing pattern. This chapter looks in some detail at the different methods of wafer fabrication used to provide the source wafers. Most of the wafers used in this thesis have been grown in an ultra-high vacuum (UHV) compatible, chemical vapour deposition (CVD) chamber, while some wafers have been produced in a gas source molecular beam epitaxy (GSMBE) chamber. In order to test the properties of a wafer it is necessary to fabricate electrically isolated devices for assessment. Most of the semiconductor wafers produced during this work required *ex-situ* processing for the fabrication of working devices. Details are given on the processing steps required in producing a device. Many of the interesting effects which occur in low dimensional semiconductor devices in a magnetic field have been described in chapter two. The electrical assessment techniques that are used to characterize samples are also explained.

3.1 Molecular Beam Epitaxy (MBE)

The most common technique used to grow wafers for research is MBE, which is a sophisticated form of vacuum evaporation allowing controlled growth of a wafer, one monolayer at a time and figure 3.1 shows a typical MBE chamber.

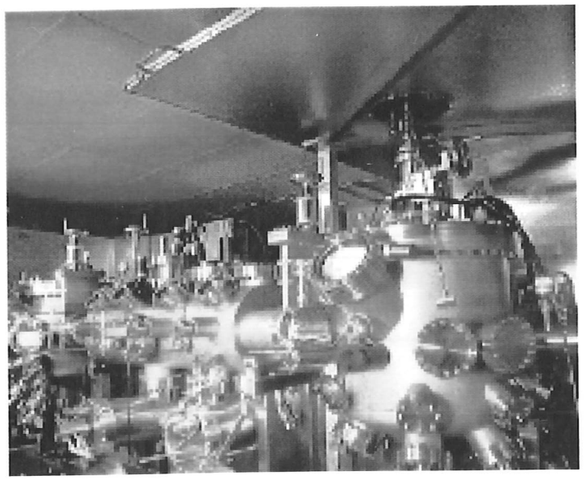

Figure 3.1: A typical MBE growth chamber (manufactured by VG Semicon).

From its inception in the early 1970s [91], MBE has been used extensively for the growth of high purity single crystals in a wide range of material systems. In MBE a source is thermally excited into producing non-interacting molecular beams of constituent elements, that are propagated without scattering across a MBE chamber until they impinge on the surface of a heated substrate.

At the substrate surface non-equilibrium thermodynamic processes compete to produce an epitaxial layer. On a clean substrate, surface atoms are free to migrate until they find a position in the crystal lattice where they can form a bond. There are usually multiple nucleation sites on the surface of the wafer and growth occurs by the spreading out of 'islands' from the nucleation sites. In very high quality material there are a large number of islands, normally with a very small height.

The temperature of the heated substrate is very important in MBE growth since this is a key factors in determining the quality of the epitaxial surface. A smoother surface can be obtained when using a high substrate temperature since atoms at the surface will have a very high mobility, resulting in greater migration, within the layers that are grown.

The rate of growth depends on the fluxes of the molecular beams, which are controlled by the evaporation rate of the material from the sources. Growth can be terminated with monolayer accuracy through the use of rapid acting shutters

that have operating speeds measured in fractions of the time needed to grow one monolayer. MBE is not a fast process and typical growth rates are around one μm an hour (roughly one atomic monolayer per second). As a result, it is very important to ensure that the impurity concentration is kept to a minimum. This is achieved by maintaining chamber base pressures of less than 10^{-11} mbar.

All SiGe growth systems suffer from Ge and dopant segregation problems since these tend to accumulate at the surface during growth. At higher temperatures there is the problem of Ge and dopant inter-diffusion, but Ge segregation can be suppressed by the presence of atomic hydrogen. This can be introduced into the growth chamber during solid source (SS) MBE [92] and can be present in gas-source growth techniques since hydrides are used as source materials (and sometimes H_2 is used as a carrier gas).

Most thermally sourced dopants for Si have a very low incorporation probability and so ion implantation is used in many systems. However high growth temperatures ($> 750°C$) are needed to anneal out the damage caused by ion implantation and this contributes to further diffusion and segregation of dopants.

One of the inherent advantages of a UHV technique like MBE is the ability to monitor growth *in-situ* during the MBE process. A combination of several systems can be utilised including reflection high energy electron diffraction (RHEED), low energy electron diffraction (LEED), auger electron spectroscopy (AES) and modulated beam mass Spectroscopy (MBMS). AES records the type of atoms present and MBMS allows the chemical species and reaction kinetics to be studied. RHEED uses forward scattering at grazing angles in order to differentiate between complete and incomplete monolayers. RHEED measurements show a minimum whenever there is a partial layer since this produces more scattering and there is a maximum whenever there is completed monolayer. As such, RHEED may be used to directly monitor growth rates since it effectively identifies individual layers as they are grown provided the growth is two-dimensional [93]. It can also reproduce the crystal structure of the surface and hence provides information about reconstructions, strain and orientation. LEED takes place in back-scattering geometry and can be used to study surface morphology, but not during growth.

3.1.1 Solid Source MBE (SSMBE)

In SSMBE, material is evaporated from solid metallic ingots either by thermally heating the source or by using an electron beam. The material travels ballistically in the UHV growth chamber and layers are defined with the use of fast switching mechanical shutters. The technique suffers from a low growth rate making it unsuitable for growing thick layers. SSMBE has been used to produce extremely high quality wafers and some of the highest mobilities for 2DEGS in the Si/SiGe material system have been produced using SSMBE [35, 94, 95, 96].

3.1.2 Gas Source MBE

GSMBE has the advantage of using room temperature sources, which reduces the amount of undesirable contaminants, especially heavy metals from electron beam evaporators. GSMBE systems have externally mounted sources that are easily replenished and it is simple to ensure that there is a continuous throughput of gas. Typical gases used are silane (SiH_4), disilane (Si_2H_6) and germane (GeH_4), as well as arsine AsH_3, phosphine (PH_3) and diborane (B_2H_6) for doping [97, 98]. One problem in using gas sources is that the rate of growth is slower than SSMBE and the role of surface hydrogen in the reaction mechanisms during growth remains unresolved.

Nominally singular Si (100) and Ge (100) substrates are cleaned using standard cleaning methods [99, 100] before the sample is loaded into the vacuum system. Prior to growth surface oxides are removed thermally by heating the substrate radiatively to 900°C (when using a Si wafer) or 700°C (when using a a Ge wafer) for 5 minutes using a SiC coated graphite heater. Temperatures are measured using an optical pyrometer. At the growth temperatures that are used, typically between 520°C to 550°C, the growth rate is limited by hydrogen dissociation, making it slower than CVD techniques.

3.2 Chemical Vapour Deposition

Traditionally researchers favour the use of MBE but this can be a slow process and CVD offers a quicker and simpler alternative. A picture of the DERA growth system and a schematic of the CVD growth system is shown in Figure 3.2 [1].

[1] The picture and the schematic used to draw Figure 3.2b were both supplied by DERA.

The growth process in CVD is similar to GSMBE, but requires a higher pressure. Normal CVD is carried out at atmospheric pressure, and involves pyrolysis of gas at an elevated temperature [101]. The chemistry involved in the growth is a combination of homogeneous (gas phase) and heterogeneous (surface) chemistry. Gas molecules incorporating Si and Ge atoms flow diffusively through the growth chamber to the substrate where they dissociate on the heated substrate and form new crystal layers. This allows the epitaxy of multiple wafers simultaneously and the growth rate can be ten times faster than MBE. Since the process does not require UHV and allows batch processing, it is the preferred method for commercial production.

Two steps in CVD growth demand high temperatures, cleaning the Si before film growth and growing a defect free film [6]. The substrate is normally heated to temperatures ranging from 900°C to greater than 1100°C in order to volatilise or desorb contaminating species such as H_2O, oxygen and carbon. A high temperature is required to remove silicon oxides which can absorb dopants (such as boron, B) from the air, as well as to maintain clean surfaces in the presence of significant contamination. It is also important to keep an oxide free surface during growth as oxygen has been shown to dramatically reduce minority carrier lifetimes in SiGe films [102]. Since oxygen is less reactive than H_2O vapour, it requires lower temperatures to maintain a clean surface and Ghidini and Smith [103] have shown that UHV is required to maintain an oxide free surface in the presence of contaminants such as H_2O.

During the growth of Si/SiGe heterostructures with CVD, if very high temperatures are required then strained materials like SiGe may suffer from strain relaxation. This in turn gives rise to more defects as well as other problems caused by lattice relaxation. High temperature growth also gives rise to layer undulations [104] which may cause distortions in the thickness of any heterostructure layers that are grown.

At high temperatures it is difficult to locate the dopant atoms accurately in the z-direction since they diffuse away from their initial position. This is made worse by Ge and dopant inter-diffusion. At low temperatures however, it is difficult for the Ge to diffuse out and three dimensional Ge islands will begin to form. As the temperature increases the Ge diffuses out until prime nucleation sites are reached and at high temperatures Ge will again start to gather and produce three dimensional structures. The dependence of the growth rate on

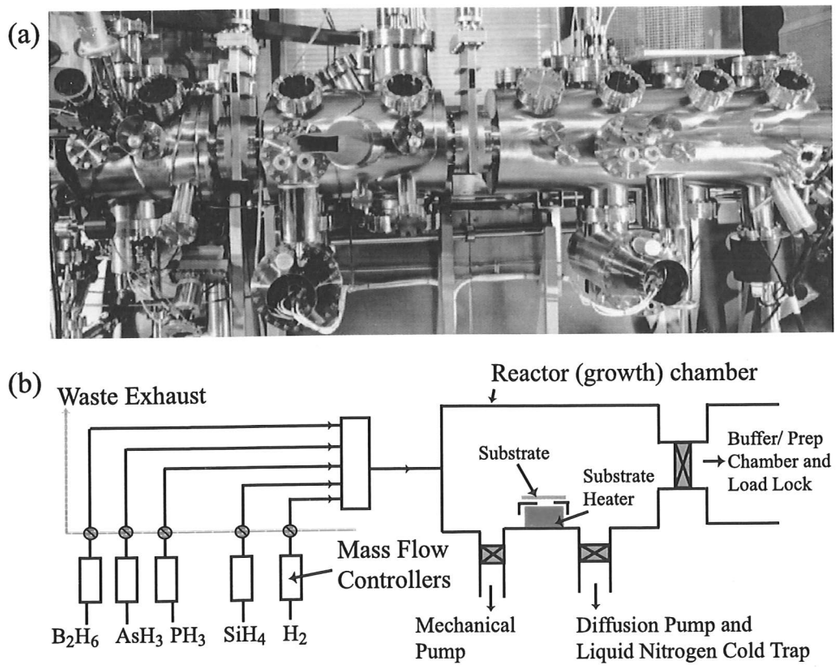

Figure 3.2: The DERA CVD growth system. (a) shows a picture of the CVD chamber and has been supplied by DERA and (b) the schematic of the UHV compatible CVD growth chamber is based on a drawings supplied by DERA, taken from the manufacturer's manual.

temperature sensitivity means that good temperature stability is required for the growth of accurate structures. To this end, many groups utilize a hot-walled growth system that heats the whole chamber in a large thermal-mass furnace and gives a greater temperature stability [105, 106].

3.2.1 Ultra-High Vacuum (UHV) CVD

Early work on Si epitaxy indicated that the number of defects in the deposited film rises dramatically as the temperature drops. However, impurities present in CVD growth, especially O, incorporate themselves into the film far more rapidly at low temperatures. In order to avoid contamination problems an extremely clean environment within the growth chamber is required. This is achieved by maintaining a low pressure in the main reactor, typically 10^{-9} mbar, to minimize the background impurity level - an approach known as UHV-CVD [107].

Doping in UHV compatible CVD systems has been demonstrated and characterised by a number of groups and for further reading see work by Meyerson [46], and Racanelli and Greeve [108].

Wafers for testing by DERA in this thesis, were all grown by CVD in a cold-walled UHV compatible stainless steel growth chamber operating with a base pressure of roughly 10^{-10} mbar [109]. The system is built inside a VG Semicon stainless steel MBE chamber modified to include a home made gas system and characterisation tools. The reactant gases used are SiH_4 and GeH_4 in a H_2 carrier gas, mixture pumped in using a Roots/rotary combination at a constant pressure, typically around 0.1 mbar. The combination of a cold-walled reaction chamber and low pressure favours heterogeneous reaction kinetics in this system and for further reading on the growth mechanisms see [110]. The system is able to use AsH_3 and B_2H_6 to provide n and p type dopants respectively. Typical DERA CVD growth is at 600°C for the strained layers and so a small degree of metastability is expected (see Section 1.4.2). However during growth, the layer thicknesses are kept well below the Matthews and Blakeslee stable thicknesses and so little or no strain relaxation is expected to occur with thermal cycling [2].

The substrate is radiantly heated by a graphite filament in close proximity to the back of the wafer, which unfortunately produces a temperature gradient from the centre to the edge of the wafer (discussed in detail in chapter five). Only one wafer at time can be produced in this system which is ideal for research since the temperature can be varied rapidly unlike many batch systems. This type of system is useful when trying to assess whether a new growth technique can be readily incorporated into a commercial fabrication process.

3.3 *Ex-situ* Sample Processing

In order to perform transport measurements, it is necessary to produce electrical contacts to the 2DEG layer. The thermally grown structures are usually only defined in the vertical direction during growth. Therefore, *ex-situ* lateral definition of a Hall bar mesa is required to enable electrical assessment of its quality.

The main features of processing which include photolithography, reactive ion etching, metallisation and annealing, are described in detail in this section. The mesa is defined by ultra violet (UV) photolithography and etching to isolate the mesa from the rest of the wafer. Ohmic contact patterns are then lithographically

[2] *private communication - Dr. A. C. Churchill, DERA*

defined before ohmic metal is deposited by evaporation. These contacts are then made electrically active using high temperature annealing of the wafer. All of the processing steps described in this section take place in a clean-room environment.

Small samples are processed, which are more manageable than whole wafers. The size of the sample depends on the size of the device and number of devices required and typically a 5 × 5 mm sample will yield four devices. The sample is cut from the wafer on a microscope mounted Karl Suss HR100 diamond tip scriber. Once the sample has been cleaved, it is cleaned using acetone and isopropanol (IPA) and finally dried with inert N_2 gas.

3.3.1 Lithography

The first step in a 2DEG/2DHG device fabrication process is the application of photoresist to the sample surface. Photoresist is a light sensitive polymer that can be formed into a thin layer, by spinning a solution of the resist on to the sample surface. Many different photoresists are available and several important factors need to be considered when selecting a resist: the wavelength response, the viscosity (which determines the range of thicknesses) and the temperature required to harden the photoresist.

The sample is placed on a chuck on a Headway Research Inc. resist spinner, where it is held in place by a vacuum. When defining a mesa a small amount of positive photosensitive resist (usually Shipley 4180M) is applied to the surface of the chip, where it is spread out evenly when the sample is spun. The recipe normally used is a rotation speed of 5500 rpm for 30 s, which leaves a uniform layer of resist approximately 1.3 μm thick.

Once the sample has been coated with photoresist it is baked on a hotplate at 105°C for 60 s. This removes any remaining solvents in the resist and increases resist adhesion to the semiconductor substrate. It is important to harden all of the resist in order to prevent an undercut profile from forming during the development stage.

A mesa pattern is then copied onto the sample using a Karl Suss MJB 3 photomask optical aligner. The optical aligner can achieve a positional accuracy of ±2 μm. Photomasks used to define the mesa are either standard Hall bar pattern masks available for use in the Semiconductor Physics Group or ones produced in-house. Once in position, the sample is brought up into hard contact with the mask (indicated by interference fringes visible in the corners of the

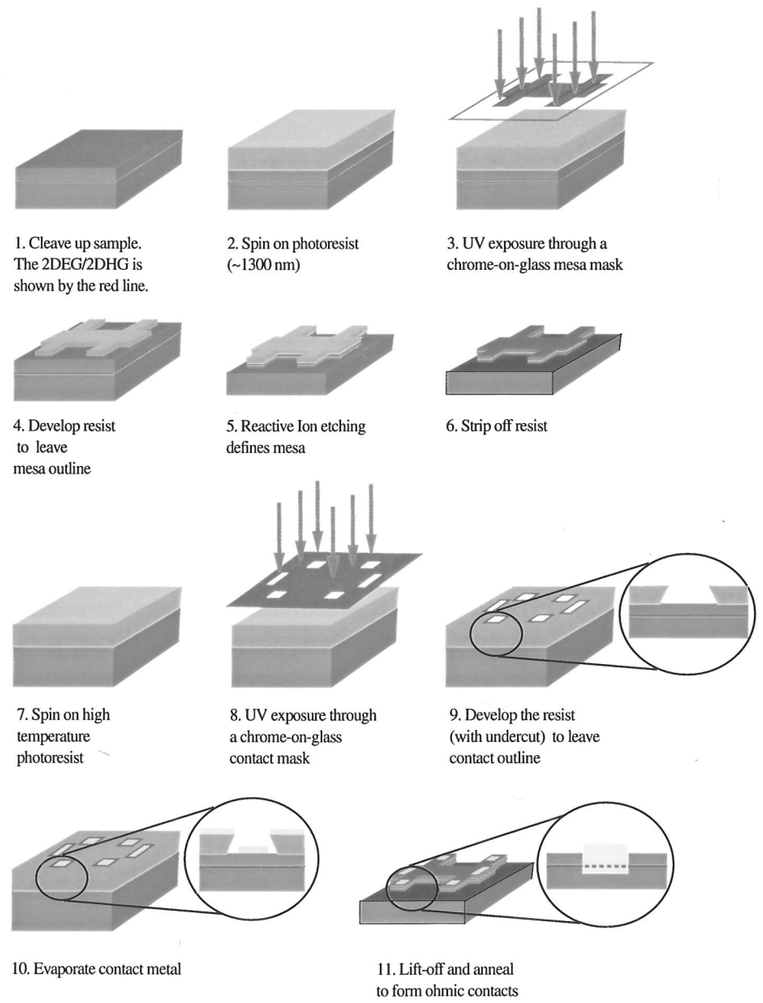

Figure 3.3: Steps involved in device processing. These are discussed in detail in sections 3.3.1, 3.3.2, 3.3.3 and 3.3.4.

sample). It is then blanket exposed to UV light (wavelength ~ 690 nm) through the chrome-on-glass stencil mask for about six seconds.

Exposure to UV light chemically alters the resist. When using a positive photoresist, such as Shipley 4180M, the regions that have been exposed to UV will be developed away leaving a Hall bar resist pattern. If a negative photoresist is used then the areas of the wafer that have been exposed to UV light will become

resistant to the developer and will remain.

After the sample has been exposed to UV, the next step is to immerse the sample in Shipley MF319 developer. The time required to fully develop the resist depends on conditions such as the photoresist quality and the humidity in the clean room. Generally the development time is determined by the duration taken for the desired pattern to become fully visible (typically 30 s). Once the sample is completely developed, it is washed in DI water and dried using N_2 gas.

The resist pattern can be inspected under an UV filtered optical microscope to ensure there has been adequate development and that there is an accurate profile. The sample can also be placed in a Sloan Technology Division Dektak 3030, which measures the resist thickness. The Dektak uses a diamond tipped force-mounted stylus to measure the height profiles on a wafer surface and can achieve a resolution of 2 nm.

3.3.2 Etching

Wet etching using acidic solutions is commonly used to remove unwanted material when processing Si or GaAs, since it causes minimal damage to the sample and gives control over the etch profiles. However, if acidic solutions are used with Si/SiGe based heterostructures, they tend to preferentially etch through strained layers leaving an undercut profile [111]. As a consequence dry etching techniques, such as reactive ion etching (RIE) are used.

To dry etch a sample, it is placed in a reactive ion etcher. An Integrate Plasma Ltd. 200E reactor that can form a CHF_3 and H_2 plasma was used[112]. The required etch depth is attained by leaving the sample for an appropriate period of time. Exposure of a Si/SiGe wafer for 20 minutes to the plasma will etch away approximately 200 nm of material. Exposure time is kept to a minimum in order to reduce damage to the sample surface. The etch rate is fairly consistent from run to run, however the chamber requires regular cleaning in order to remove any polymer deposition. After the etching process, the Dektak can be used again to measure the pattern height on the etched surface and subtracting the thickness of the photoresist layer from the total height will determine an approximate etch depth. It should be noted that the photoresist will also be etched.

After the etching process has been completed, the photoresist layer can then be stripped off by washing the sample in acetone, followed by IPA.

3.3.3 Ohmic Contacts

Ohmic contacts are required in semiconductor processing to allow electric currents to flow in and out of the device. The ohmic contact dopes the crystal in a localized area leaving a column of n-type or p-type material down to the 2DEG/2DHG. The current-voltage relationship should be linear and the contacts should remain ohmic at low temperatures and high magnetic fields.

To form an ohmic contact, metal needs to be first deposited onto the sample surface. Shipley 1813 photoresist is spun on to the surface and then baked at a temperature of 100°C for 60 s in order to aid adhesion. It is then exposed to UV light for 6 s on the optical aligner, through a chrome-plated photo mask with the ohmic contact pattern aligned to the existing mesa.

Prior to development, the sample is immersed in chlorobenzene for 2 minutes in order to harden the surface of the polymeric coating resist. This enables an undercut profile to be produced, since development of hardened resist at the surface is slower than the development at the sides. An insufficient undercut leads to problems after the completion of the ohmic metallisation, since the metal may have formed a continuous layer over the resist and SiGe surface and so the lift-off process may not occur.

After the chlorobenzene immersion, the sample is developed and rinsed in DI water and dried in N_2. The developed region may have traces of photoresist in the contact areas. To ensure that there is a good metal-semiconductor contact the Si surface needs be free of contaminants. To remove the remains of any unwanted photoresist, the sample is exposed to a microwave induced oxygen plasma for 30 s in an Oxygen Barrel Plasma Etcher.

As mentioned earlier, Si has a thin native oxide that may impede the diffusion of contact metal. To remove this surface oxide the sample is etched in a dilute HF solution (10% HF: 90% H_20) for 30 s. This solution etches the oxide but does not attack Si/SiGe.

The sample is loaded into an Edwards E306A evaporator and is clamped into position over tungsten boats that contain metal for the ohmic metal deposition. To ensure low impurity incorporation during the deposition process, the evaporator is pumped down to a low pressure ($\sim 10^{-6}$ mbar) before evaporation is commenced.

The metal chosen for contacts must contain an appropriate doping material. For n-type ohmic contacts, a few pieces of Au (1% Sb) and NiCr are placed in

separate tungsten (W) boats, which are resistively heated until the metal starts to evaporate. Usually an alloy of 100 nm Au (1% Sb)/ 20 nm NiCr/ 60 nm Au (1% Sb) is deposited. The small amount of NiCr acts as a diffusive-barrier, which helps ensure that there is enough Au left to form a bond pad after annealing, since Au diffuses rapidly in Si. P-type contacts are formed by a similar evaporation process of Al (1% Si), with Al acting as both the dopant and the bond pad. The 1% Si prevents the semiconductor from out-diffusing into the metal and improves the contact morphology.

3.3.4 Lift-off and Annealing

After the evaporation process, any unwanted metal is lifted-off together with the photoresist by immersing the sample in acetone for about 5 minutes. Only regions where metal was evaporated directly onto the SiGe surface will remain coated. If the deposited metal layer is thicker than the resist layer then the entire sample will be covered in metal and the resist is unable to lift-off.

Low resistance electrical contacts are made between the deposited metal and the 2DEG/2DHG by annealing the sample in an atmosphere of N_2 and H_2 at 400°C for 600 s. The samples are placed in a Leisk annealer under a flow of forming gas (10:1 N_2:H_2) to expel any O_2 from the system. Quartz lamps are used to heat the samples. During the anneal the surface metal will penetrate into the sample and will 'spike' down producing degenerately doped SiGe and will form a low-resistance conducting path from the surface to the active layers. A thin Schottky barrier is formed between the surface metal and the heavily doped SiGe below it such that electrons/holes are able to tunnel through, thus forming an ohmic contact [113].

Repeating a similar procedure to one described above for ohmic contacts can be used to make surface gates, however it is important to note that surface gates are not annealed since it is important to not diffuse any metal into the semiconductor for the formation of a Schottky barrier.

3.3.5 Device Packaging

To check that the processing steps have been successful the sample can be tested on a Karl Suss probe station at room temperature (RT) and 77 K. The sample is then cut into small 2 × 2 mm devices using a microscope mounted Karl Suss HR100 scriber.

To facilitate easy handling and electrical measurements in a cryostat, each small device is fixed on to a ceramic leadless chip carrier (LCC) package. All of the probe arms for the various cryostats described in this thesis, use a charntek connection. This enables the chip package to be connected to the wiring loom of the probe giving a good electrical connection without soldering.

The device is held on to the LCC charntek package with glue such as silver dag. The glue needs to be a metallic compound that can conduct and so can form an electrical connection to the substrate. Electrical connections are made between the ohmic contact pads on the device and the package using Au thread on a Kulicke and Soffa 4121 ball bonder. The bonder attaches two ends of a thin Au wire to the contacts using an ultrasonic pulse. The Au wire will readily bond to both Au and Al, but when using other metals sometimes it is useful to evaporate a thin layer of NiCr and Au to facilitate the bonding of the Au wire to the ohmic contacts.

3.4 Electrical Characterisation

For materials with high mobilities, effects such as the Quantum Hall effect and Shubnikov-de Haas oscillations can be seen by applying a constant current across a sample and then measuring the voltage drop across it (see also [52, 114]). A Hall bar geometry is commonly used for the electrical assessment of semiconductor material quality and has been used for most of the devices produced in this work. The Hall bar configuration allows four-terminal measurements to be undertaken, which removes the unwanted contribution of any contact and spreading resistances from the measurement [115].

In the standard assessment set-up, a constant AC current is passed between two contacts along the Hall bar. These current-carrying probes will still have a contact resistance (due to the metal and semiconductor interface) and a spreading resistance (encountered by the current when it flows from the metal into the semiconductor) associated with them. Two separate inner contacts measure the longitudinal voltage. By measuring a voltage across between the two current contacts, only the resistance between the two voltage probes is measured, removing contact and spreading resistances.

Figure 3.4 shows diagrammatically the configuration utilised for measurements at both 77 K and 1.5 K. All measurements are carried out using phase

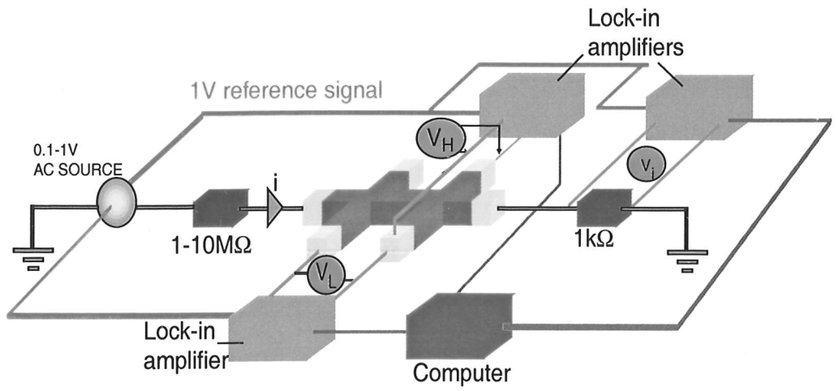

Figure 3.4: Configuration used at 77 K and 1.5 K for electrical characterisation.

sensitive AC lock-in techniques, which allow the isolation of weak output measurement signals from a high level of background noise. This is essential as the currents used are very small (about 100 nA) to avoid ohmic heating effects in the device. With low-level currents, DC measurements are problematic due to the large background noise and unavoidable DC offsets (such as those due to the thermoelectric effect). The noise can be reduced using thin co-axial cables or twisted pairs.

An oscillator is used to provide a low frequency 1 V rms AC voltage signal (usually with a frequency less than 100 Hz). A current limiting resistor (10 MΩ) is used to set the current through the device at 100 nA and it is assumed that the resistance of the device is small compared to the series resistor. Voltage measurements on Stanford SR510 lock-ins are referenced to the oscillator frequency and measurements are made with all contact probes to check that the readings are symmetrical across the device.

The parameters of interest are usually the Hall coefficient and the carrier mobility of the devices. The carrier concentration, (deduced from the Hall resistance) and the sheet resistance can be used to quickly find the mobility of the sample. The 2D Sheet Resistance, ρ_s of the devices is:

$$\rho_s = \frac{WV_L}{LI} \tag{3.1}$$

where W is the Hall bar width, L is the Hall bar length, V_L is the longitudinal

voltage and I is the current through the device. The Hall voltage V_H, (measured directly) gives a Hall resistance of:

$$R_H = \frac{V_H}{BI} \tag{3.2}$$

where B is the strength of the magnetic field. This gives a carrier concentration, n_s of:

$$n_s = \frac{1}{e^- R_H} \tag{3.3}$$

These are used to calculate the mobility, μ:

$$\mu = \frac{L}{We^- n_s \rho_s} \tag{3.4}$$

All voltage and current measurements are recorded using an Acorn A5000 computer with 'Cryomeas', a piece of control and data acquisition software, written and compiled by Dr. C. J. B. Ford of the Semiconductor Physics Group. During the device preparation stage, multiple ohmic contacts are produced on any one device, so that 4-terminal measurements are possible even if some ohmic contacts fail.

The 1.5 K cryostat sample probe, which holds the LCC package, is also equipped with a red LED for illumination of the device while at low temperatures. Illumination may excite electrons from deep donor states (or generate electron-hole pairs) in the SiGe layer and enhance the conductivity of the 2DEG in some samples. The enhancement in carrier density remains even after the illumination is switched off. This persistent photoconductivity effect is sometimes required to produce a conducting 2DEG if there are an insufficient number of carriers in the channel for conduction in the dark.

For some devices, DC voltages can be applied to a surface Schottky gate using a Keithley 236 Source Measuring Unit (SMU) which is capable of sourcing DC voltages while measuring leakage currents or vice versa. The SMU can supply large voltages and currents and can also be configured to have a compliance rating which limits the applied voltage when the maximum current setting is exceeded. This should help to avoid a large current flow and sudden ohmic heating of the device.

3.5 Cryogenic Measurement Systems

The bulk of the assessment of the devices presented in this thesis involves low-temperature electrical measurements at 1.5 K in a Helium^4 (^{4}He) cryostat.

3.5.1 Helium^4 Cryostat

A ^{4}He cryostat fitted with a superconducting solenoid magnet capable of reaching 10 T fields has been used for the majority of measurements at low temperatures. A schematic of the Helium^4 cryostat used for assessment is shown in Figure 3.5. By using a rotary pump the pressure of the chamber containing the liquid He is reduced and temperatures down to 1.5 K can be obtained.

The sample is held at the end of a probe, which is lowered into a sample space at the bottom of a thermally insulated vacuum column in the cryostat. A shell containing liquid ^{4}He surrounds this. The helium can be fed from the main bath into the sample space by a needle valve. Outside the ^{4}He bath the cryostat has a vacuum jacket and an outer shell that is filled with liquid N_2 to limit boil-off. The cryostat needs a liquid N_2 and liquid ^{4}He refill every 20 to 40 hours depending on the magnet use.

Once filled with liquid ^{4}He the sample space can reach temperatures of around 4.2 K; the atmospheric boiling point of liquid ^{4}He. This can be reduced further to 1.5 K by pumping on the sample space to change the pressure. Changing the pumping rate can control the temperature below 4.2 K but for higher tempera-

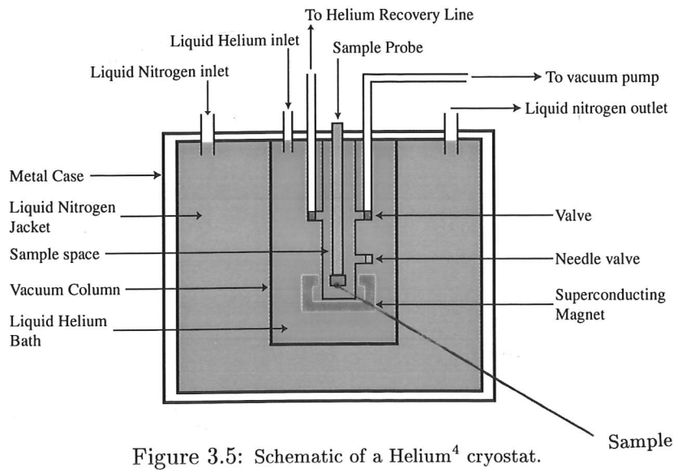

Figure 3.5: Schematic of a Helium^4 cryostat.

tures a heater at the end of the probe can be used. The temperature that the sample is held at is measured by the use of a previously calibrated resistance thermometer.

3.5.2 Dipping Dewar

A sample is mounted on the end of a probe and is inserted into the dewar containing liquid ^{4}He. The dewar has an insulating vacuum jacket to help minimize boil-off. The sample will remain at 4 K, which is sufficiently low enough for conduction in the doping layer of the sample to be frozen out. This permits the testing of the ohmic contacts to the 2D layer and allows the characterisation of the gate-leakage.

3.6 Alternative Measurement Techniques

Many measurement techniques can be employed after the growth process to obtain useful data about SiGe heterostructures and wafers. These include capacitance-voltage (CV) profiling [116] which can be used to measure the carrier concentration profile in a sample and electron beam induced current (EBIC) imaging which is a useful method for imaging dislocation densities [39]. Photoluminescence (PL) measurements provide a nondestructive technique for studying defects and obtaining impurity concentrations [117], while Raman scattering may be used to measure layer thicknesses [118] and x-ray diffraction which is the main technique used to measure strain in the SiGe system [119].

Whilst all of these techniques can be used to yield valuable information only the following few are described below in detail, transmission electron microscopy (TEM), secondary ion mass spectrometry (SIMS) and atomic force microscopy (AFM). These are the ones that have been utilised the most during the course of this thesis.

3.6.1 Transmission Electron Microscopy

Transmission electron microscopy passes high-energy electrons into a material, which will then diffract and scatter off the ion core potentials of solids as they pass through thin (0.1 μm) layers. TEM provides near atomic resolution with enough contrast between Si and Ge to provide an accurate profile [120]. Dislocations may be imaged quite easily but it is difficult to determine accurate dislocation

densities over large volumes since the resolution is too high. Whilst TEM is a useful tool for analysis of initial wafer structures, especially with thin strained layers, it is a destructive technique requiring very thin samples (<100 μm thick). All TEM images used in this thesis were taken by David Wallis at DERA.

3.6.2 Secondary Ion Mass Spectrometry

Secondary ion mass spectrometry is a powerful technique for analysing small volumes of non-volatile material [121] and is one of the main techniques used to check the dopant profiles/concentrations and Ge profiles/concentrations of grown material.

SIMS involves in-vacuo bombardment of a small specimen (a few cm^2) with a primary focused ion beam in the energy range 1 keV to 20 keV. The ion beam sputters away the sample at the surface, which means that it is a destructive technique. The secondary ions, characteristic of the sample, are collected and analysed using a mass spectrometer and are identified by their mass/charge ratio. Since 90% of the secondary ions are emitted from the outer two atomic layers of the sample, the technique can be surface sensitive. Data may be stored as a 'stack' of images so that profiles and sections may be extracted.

SIMS can provide chemical information down to levels of 1 atom in 10^{10}, in favourable circumstances, however both depth resolution and accuracy degrade with increasing depth due to effects such as atomic displacement and ion mixing. SIMS can be used to give an accurate dopant and Ge depth profile down a few nm [122]. All SIMS measurements used in this thesis, were performed by Alan Pidduck at DERA.

3.6.3 Atomic Force Microscopy

Atomic Force Microscopy is the main technique used to investigate the surface and interface morphology in SiGe wafers accurately down to the nm scale [104]. AFM involves the scanning of a probe across a surface to obtain 3D information about the surface. AFM images are obtained by measuring the force developed on a sharp tip when it is in close proximity to a sample surface.

The AFM used in this work was a Digital Instruments Inc. Dimensions 3000 system, which operates in atmospheric conditions. This is highly sensitive system which allows atomic level surface features to be distinguished over relatively large

scan areas. For more details see the Digital Instruments Inc. AFM system manual [123]. The AFM images used in this thesis have been taken by Drs. Neil Curson and Patrick See at the Semiconductor Physics Group.

AFM images can give highly useful information about the surface morphology and in research carried out by Kiehl *et al.* [120], there is evidence that suggests that there will be a strong increase in surface clustering and surface roughness as the Ge content is increased.

Chapter Summary

This chapter provides a brief review of the growth systems that have been used to provide wafers during the course of this thesis, discussing both MBE and CVD techniques. The *ex-situ* sample processing routine that is used to provide Hall bar devices for electrical assessment of material quality has been presented in Section 3.3 and details of each processing stage have been outlines. There is brief review of the set-up that is used for 4-terminal Hall bar electrical characterisation of fabricated devices when obtaining the Hall mobility and carrier density. The final section outlines the SIMS, TEM and AFM techniques that have been used to provide details of wafer structure and surface morphology.

Chapter 4

Two Dimensional Devices

4.1 Introduction

This chapter examines some of the Si/SiGe samples that have been used to characterise both 2DHGs as well as 2DEGs wafers. Since 2DEG samples in the Si/SiGe system often display superior transport mobilities when compared to Si/SiGe 2DHGs [15, 16, 18, 19], most of the work in this thesis has been carried out with 2DEGs. Hence only a small section on Si/SiGe 2DHGs is included. Section 4.2 presents a brief overview as well as covering the structure and low temperature transport properties of some typical Si/SiGe 2DHGs samples.

The majority of the samples studied during the course of this thesis are Si/SiGe 2DEGs that do not have a conventional structure. Hence only a brief overview of a typical conventional Si/SiGe 2DEG structure as well as its low-temperature transport properties has been included in Section 4.3.

When using Si/SiGe 2DEGs that do not have a step graded buffer, samples with performances comparable to Si/SiGe 2DHGs are produced. The best low temperature mobilities are only 17 000 $cm^2V^{-1}s^{-1}$ [124]. Optimum performances of n-type MODFETs in the Si/SiGe system are from wafers that have a tensile strained Si quantum well on a relaxed $Si_{1-x}Ge_x$ (typically $0.2 < x < 0.4$) virtual substrate [14].

The vast majority of present day SiGe 2DEGs have a step graded virtual substrate in order to minimize the threading dislocation density. Most structures that have a virtual substrate will have a thick uniform SiGe layer on top of which the desired heterolayers are grown. Previously virtual substrates have not been treated as normal Si substrates and the complete wafer structure is normally

grown in a one step process. Any steps involving any *ex-situ* processing during wafer growth are usually avoided. The wafer remains *in-situ* in UHV conditions and thus the risk of impurity contamination is minimized. If at any point the growth run is stopped and later restarted, it has the effect of forming a regrowth interface at the point where normal growth resumes. It was believed that the inclusion of a regrowth interface would have an adverse effect on the material properties of the wafer. The interface would have a rougher surface, and hence there would be increased interface roughness scattering and the possibility of electron traps forming at the interface further degrading the electronic transport properties.

Gas based growth systems suffer from dopant segregation (and memory) problems when using the n-type dopants required to form SiGe 2DEGs [125]. The presence of background dopants within the chamber, caused by previous growth runs, can lead to a contamination of a growth wafer.

In Section 4.4 it will be shown that it may be possible to *ex-situ* clean the wafer and that is possible to include a regrowth interface within a wafer without seriously degrading the material properties. A new growth technique is used that involves the growth of a virtual substrate, which is subsequently removed from an UHV compatible CVD growth chamber. Following a chemical clean the wafer is returned to the growth system in order to fabricate any additional layers, such as the modulation doped layers for 2DEG structures. The effects of using this technique on the electrical properties are presented in Section 4.4. Results from this section also been presented in two papers (see [126] and [127]).

4.2 Conventional Si/SiGe 2-Dimensional Hole Gases (2DHGs)

2DHGs are relatively simple to produce in the Si/SiGe system. The valence band edges are always at higher energies in SiGe when compared with Si, regardless of the strain conditions. The size of the valence band offset between Si and Ge is taken to be $0.74x$ eV, where x is the Ge fraction.

Most early research on modulation-doped Si/SiGe heterostructures centred on 2DHGs. Initially very promising mobilities were obtained that were superior to p-type Si MOSFETs [128]. Despite the continuing research in 2DHGs systems, they have been overtaken in terms of performance and mobilities by SiGe 2DEGs

and remain considerably worse than 2DHGs in other material systems like GaAs.

Si/SiGe virtual substrate 2DHGs have been grown which have mobilities of 55 000 $cm^2V^{-1}s^{-1}$ at 4.2 K [19]. These mobilities have been obtained using strained Ge channels. If pure Ge channels are used the lattice constants are so mismatched that pseudomorphic growth cannot occur beyond a few monolayers and so the active region needs to be on a virtual substrate [16,19].

There have been many papers that discuss the limitations of 2DHGs in the Si/SiGe system [50,129,130,131,132] but there is still doubt as to which is the dominant scattering mechanism. Whilst alloy scattering is often regarded as being the main limiting factor, it could also be charged interface impurity scattering or interface roughness scattering [19,133]. Charged interface scattering may be limited by higher temperature growth [96], but this requires a lower Ge fraction in the alloy in order to try and prevent strain relaxation. Alloy scattering places a theoretical maximum low temperature mobility of 30 000 to 100 000 $cm^2V^{-1}s^{-1}$ [129,131].

Several authors have discussed the relationship between the hole effective masses and Ge concentration. It has been shown that samples with a higher Ge fraction will have a lower effective mass, which gives an increase in mobility [134, 135]. However as the Ge concentration is increased, the width of the SiGe channel has to decrease in order to prevent strain relaxation and high Ge concentration virtual substrates are also required.

4.2.1 Conventional Si/SiGe 2DHG Sample Structure

A typical SiGe 2DHG structure is shown in Figure 4.1. A thick undoped Si buffer is grown on top of a n-Si(100) substrate. There is a variable channel thickness and Ge fraction within the SiGe channel. A thin i-Si spacer is grown on the SiGe channel before a p-type Si region is grown. Only a few 2DHG wafers were received during the course of this thesis. All of the devices that were tested had poorer mobilities and displayed poor transport properties when compared to the 2DEGs.

Typical magnetotransport measurement data for a p-type modulation doped Si/SiGe heterostructure are shown in figure 4.2. The longitudinal (ρ_{xx}) and Hall resistivity (ρ_{xy}) in perpendicular magnetic fields up to 8 T is shown for

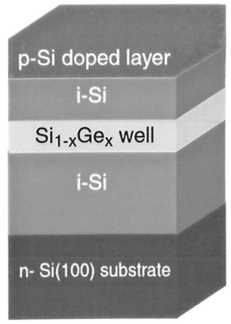

Figure 4.1: A typical 2DHG structure in the Si/SiGe system

samples taken from a DERA 2DHG wafer. Mobilities of around 4000 $cm^2V^{-1}s^{-1}$ for carrier densities of $\sim 4.8 \times 10^{11}$ cm^{-2} at 1.5 K are measured. Despite the rather poor mobility, the samples show well-defined Shubnikov-de Haas (SdH) oscillations in ρ_{xx} and quantum Hall effect plateaux are evident in ρ_{xy}. SdH oscillations and the quantised Hall effect is clearly evident in both samples, with better defined plateaux at higher fields.

Measurements with higher quality samples at fields of 14 T and at a lower temperature of 50 mK, reveal that Shubnikov-de Haas oscillations develop clear zeros ρ_{xx} at filling factors of $\nu = 1$, 2 and 3. The quantised Hall effect can also be observed at these filling factors with well-defined plateaux in ρ_{xy}. [For further information and reading on Si/SiGe 2DHGs see [20, 58]]

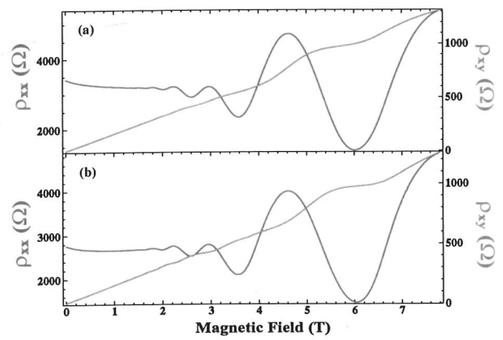

Figure 4.2: Longitudinal (ρ_{xx}) and Hall resistivity (ρ_{xy}) in perpendicular magnetic fields up to 8 T at 1.5 K, for samples from DERA Si/SiGe 2DHGs are shown. Shubnikov-de Haas oscillations and quantum Hall effect plateaux can be seen.

4.3 Conventional Si/SiGe 2-Dimensional Electron Gases (2DEGs)

In order to form a conduction band offset a relaxed SiGe buffer is required. If a strained Si channel is grown between two relaxed SiGe layers, then there will be a conduction band offset of $0.6x$ eV producing a quantum well in the Si layer. This will allow the formation of a 2DEG within the strained Si.

The structure used to form a typical Si/SiGe 2DEG is shown in Figure 4.3 to remove the effects of remote dislocation scattering at low temperature. In most wafers a thick constant composition buffer is grown on top of the virtual substrate. A thin, strained i-Si channel forms the quantum well, the thickness of which is limited by concerns over strain relaxation. Next, a Si/SiGe spacer is grown before the wafer is doped with n-type dopants such as As or P. Finally the wafer is capped with a thin i-Si layer.

Strain in a strained Si quantum well, will lift the valley degeneracy, which will suppress inter-valley electron scattering with the in-plane effective mass remaining constant [58, 136] One distinct advantage is that because of the pure Si channel there should be reduced alloy scattering and the main limiting scattering mechanism for the mobility is considered to be remote ionised impurity scattering (assuming that other sources of disorder have been sufficiently reduced). There have been several investigations into the types of scattering mechanisms and the effect they have on a Si/SiGe 2DEG in order to try to determine what should limit the mobility.

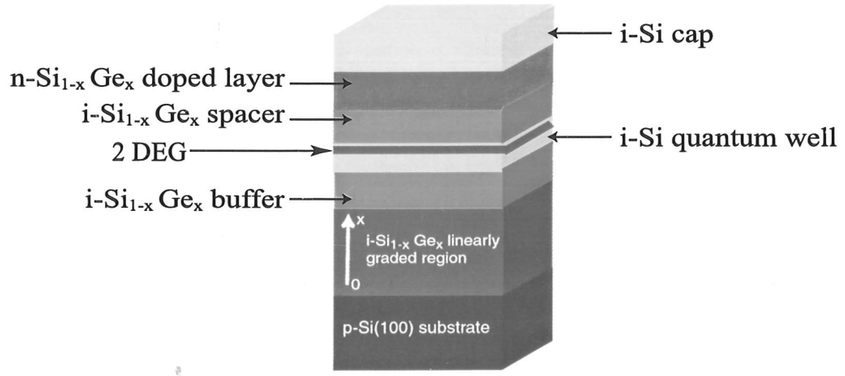

Figure 4.3: A typical 2DEG structure in the Si/SiGe system

Background impurity scattering and remote impurities in the doping layer were identified by Stern and Laux [137] as important factors. Alloy scattering due to segregation of Ge into the well was predicted to be small while interface roughness was shown to be a possible limiting factor. Mechanisms such as the influence of threading dislocation densities (which are not expected to have a significant effect at readily attainable densities) and strain from the graded buffer (which ought to be filtered by sufficiently thick constant composition layers) were considered by Monroe *et al.* [138]. They found no fundamental barrier to mobilities, which are predominantly limited by remote ionised impurity scattering in these systems and so very high electron mobilities should be possible. The highest electron mobility reported for SiGe virtual substrates is 390 000 $cm^2V^{-1}s^{-1}$ at 400 mK. It is possible to enhance the conduction with the careful use of surface and back gates to move the electron wavefunction away from the heterointerface and achieve a mobilities of up to 520 000 $cm^2V^{-1}s^{-1}$ [18]. While these values remain considerably lower than their counterparts within III-V material systems such as GaAs/AlGaAs, they are far superior to n-Si MOSFETs.

4.4 Si/SiGe 2DEG Wafers with a Regrowth Interface

This section investigates the effect of removing a grown SiGe virtual substrate from an UHV compatible CVD growth chamber, cleaning the virtual substrate using standard Si cleaning technology and replacing the wafer into the growth system to regrow device heterolayers. To successfully produce a wafer that has an *ex-situ* chemical clean, a slightly different wafer production process is needed, compared to the normal wafer growth process. The process incorporating a regrowth layer is detailed in Figure 4.4.

4.4.1 Comparison of Si/SiGe 2DEG Wafers 6B121 and 6B122

To investigate the effects of the inclusion of a regrowth interface on the transport properties, two nearly identical wafers were grown by DERA, wafers 6B121 and 6B122. Both were grown in the UHV compatible CVD system described in Section 3.2.1. Wafer 6B121 was taken out the growth of the UHV compatible CVD chamber after the growth of the relaxed SiGe substrate and chemically cleaned before being returned to the chamber. 6B122 did not have any chemical

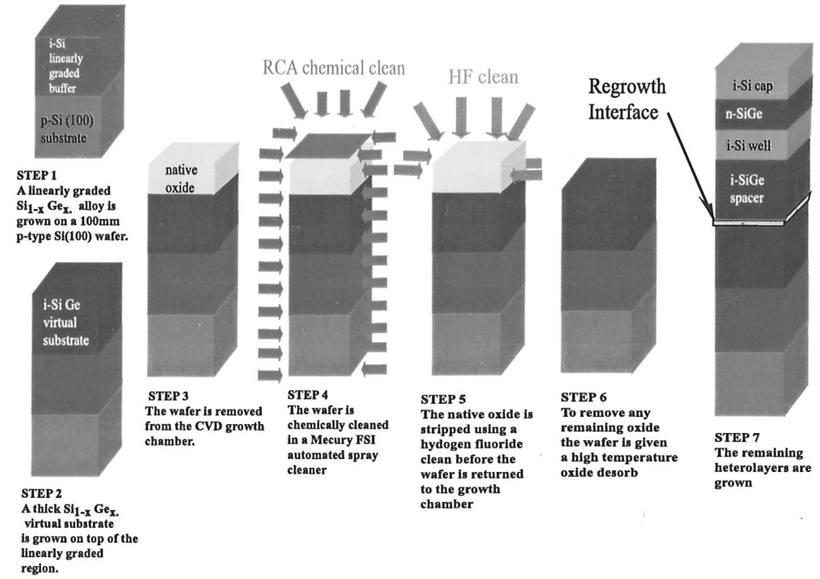

Figure 4.4: The wafer fabrication process incorporating a regrowth interface.

clean and was produced in a single step process. The differences in the two structures are illustrated in Figure 4.5.

Structure of Wafers 6B121 and 6B122

Both wafers had 100 mm diameter p-Si(100) substrates on top of which a linearly graded SiGe alloy was grown. The wafers were initially graded to 25% Ge over 4.2 μm. After growing a suitably thick i-$Si_{0.75}Ge_{0.25}$ constant composition layer, the Ge fraction, x, was stepped down to 23%. In wafer 6B122 the 241 nm of i-$Si_{0.77}Ge_{0.23}$ growth was uninterrupted. The growth of wafer 6B121 was interrupted after 100 nm and the wafer was given an *ex-situ* chemical clean before it was returned to the UHV compatible CVD chamber, where another 127 nm of i-$Si_{0.77}Ge_{0.23}$ was deposited. The initial growth was all carried out at a temperature of 800°C.

6B121 was chemically cleaned in a Mercury automated spray cleaner (manufactured by FSI) with a B/CLEAN/R2 clean recipe. A B/CLEAN/R2 recipe consists of the following cleans in sequence; hot H_2O:H_2SO_4, cold H_2O:HF, hot H_2O:H_2O_2:HN_4OH and finally hot H_2O:H_2O_2:HCl, with hot (80°C) rinses and

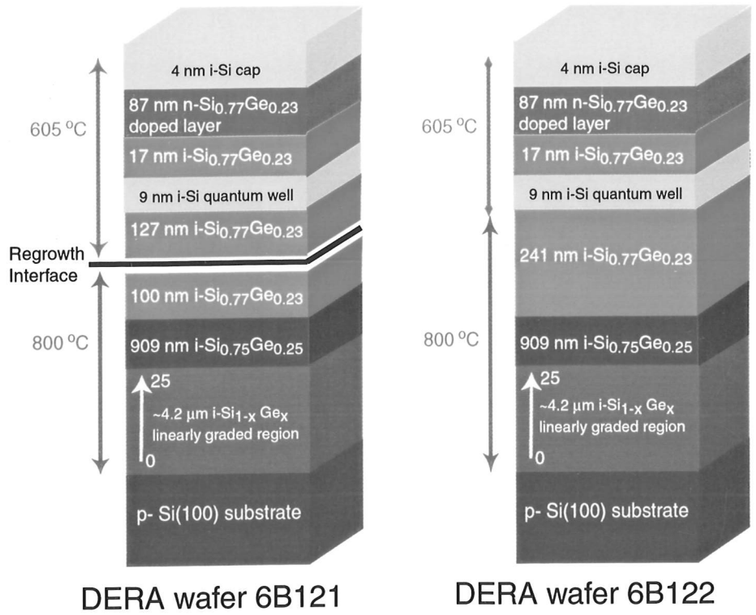

Figure 4.5: Structure of DERA Si/SiGe 2DEG wafers 6B121 and 6B122.These have a near identical structure but 6B121 has a regrowth interface.

cold water (20°C) rinses between each clean. This cleaning recipe terminates the surface with a thin, chemical oxide. A HF clean is required to remove this oxide before the wafer is replaced in the growth chamber.

Once the wafer is returned to the CVD chamber, any residual oxide needs to be removed with a high temperature oxide desorb before normal growth can resume. Upon its return to the UHV compatible CVD system, 6B121 was heated to 880°C in 130 Pa atmosphere of H_2 to remove any passivating chemical oxide.

The remaining heterolayers were identical in both wafers and were grown at pressure of around 20 Pa at a temperature of 605°C. The quantum well in both wafers was a 9 nm thick undoped Si layer. Before the wafers were doped, a 17 nm undoped $Si_{0.77}Ge_{0.23}$ spacer was deposited. Then an 87 nm n-type $Si_{0.77}Ge_{0.23}$ layer was formed by interrupting the SiGe growth while exposing the surface to 1000 ppm AsH_3:H_2 gas for 60 s (leaving an arsenic, As, rich layer at the interrupt) and then resuming the growth. SIMS subsequently established a uniform dopant concentration to be about 5×10^{18} cm^{-3}. The wafer was capped with a nominal 4 nm thick Si layer. Samples from the centre of each wafer were processed as

described in Section 3.3 and annealed Au (1% Sb)/NiCr/ Au (1% Sb) metal was used for the n-type ohmic contacts.

Magnetotransport Results from Wafers 6B121 and 6B122

Figure 4.6 shows the longitudinal (ρ_{xx}) and Hall resistivity (ρ_{xy}) in perpendicular magnetic fields up to 8 T for samples from 6B121 and 6B122. The samples show well-defined Shubnikov-de Haas (SdH) oscillations in ρ_{xx}. Figure 4.6 shows that the sample without a regrowth interface is a higher quality sample with better defined quantum Hall effect plateaux and SdH oscillations. Samples from wafer 6B122 display a mobility of 203 000 $cm^2V^{-1}s^{-1}$ for a carrier density of 3.7×10^{11} cm^{-2}. Samples from wafer 6B121, which have a regrowth interface, display a lower mobility of 133 000 $cm^2V^{-1}s^{-1}$ for a carrier density of 3.3×10^{11} cm^{-2}

It is clear that it is possible to produce wafers with a regrowth interface that are able to conduct at low temperatures. The regrowth interface has a clear effect on the transport properties. There is a reduced carrier density in

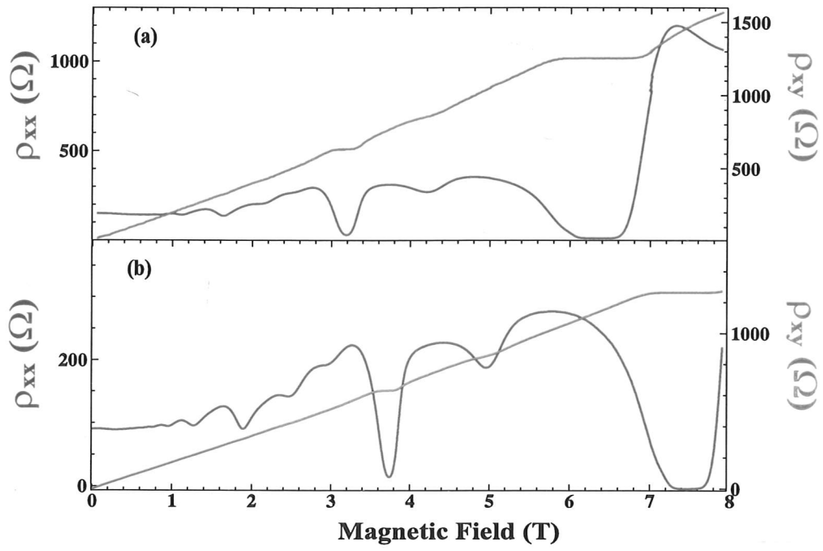

Figure 4.6: Magnetotransport measurements taken in perpendicular magnetic fields up to 8T, for samples from DERA Si/SiGe 2DEGs wafers. Sample (a) is from wafer 6B121 and has a regrowth interface, whilst sample (b) is from wafer 6B122 and has no regrowth interface. Well-defined Shubnikov-de Haas oscillations and quantum Hall effect plateaux can be seen.

wafer 6B121 (with regrowth interface) compared to 6B122 (without regrowth interface) by a factor of 0.9 at 1.5 K. The presence of trapped charge present at the interface would account for this decrease in carrier density. There may be strain relaxation associated with the inclusion of the regrowth interface that would lead to introduction of dislocations, which would affect the mobility. It is more probable that the introduction of a regrowth interface leads to a rougher surface as well as causing an increase in interface roughness scattering. The mobility in the sample with a regrowth interface is 65% of the samples without the interface at 1.5 K. 6B121 still has a very high mobility and the next section explores the effect on a regrowth interface on the transport properties in more detail.

4.4.2 Investigation of the Effect of Adding a Regrowth Interface

In order to more fully investigate the effect of adding a regrowth interface a series of six modulation-doped 2DEG wafers were grown by DERA, the 7B series, in the same UHV compatible CVD system used to produce 6B121 and 6B122. The 7B series wafers all have a fairly similar structure to wafer 6B121, with only minor differences. All of these wafers were 100 mm diameter p^- Si(100) substrates on which a linearly graded SiGe alloy was grown. These virtual substrates were grown at 800°C and consisted of an undoped, linearly graded buffer and an undoped, thick uniform SiGe layer.

4.4.3 7B Series Wafer Growth

Four wafers were graded from 0% to 23%, followed by a thick $Si_{0.77}Ge_{0.23}$ constant composition virtual substrate (series A). The grading in the remaining two wafers was the same as 6B121, with Ge grading to 25% followed by a step down to 23% in the constant buffer region of the virtual substrate (series B). Figure 4.7 depicts the alloy concentration as a function of growth time for the both series A and B as well as the structure of the later heterolayers. The linearly graded region in both series was typically about 4 μm thick, graded at a rate of about 8% Ge per μm. On top, a thick i-$Si_{0.77}Ge_{0.23}$ constant composition layer was grown in both series, typically between 1 to 1.5 μm thick. The two different series were used in order to compare wafers with matched virtual substrates to those with a mismatch.

As with wafer 6B121, once a suitable virtual substrate had been grown, the

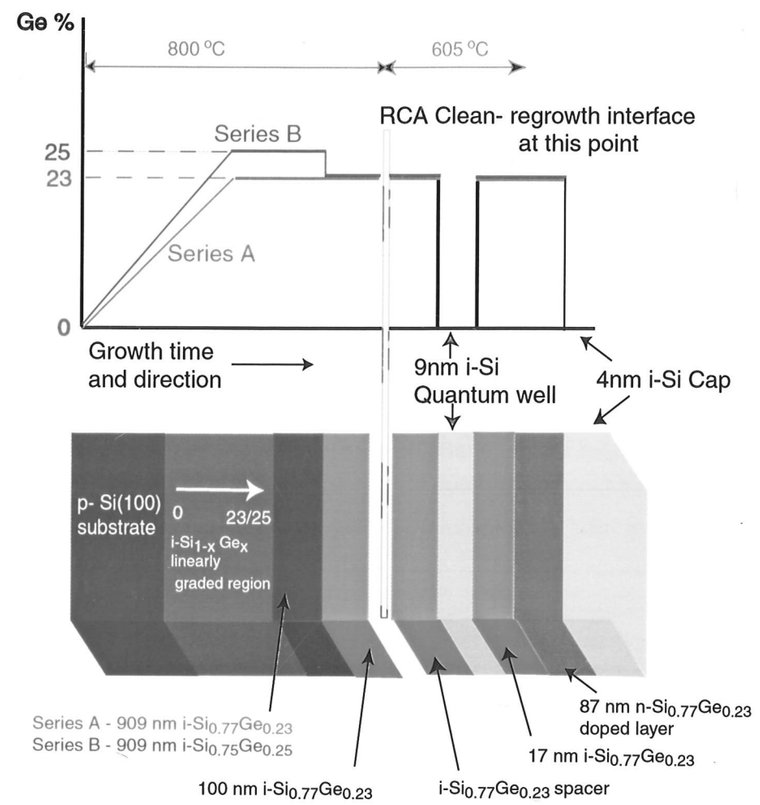

Figure 4.7: DERA 7B series growth summary. All of these wafers have a regrowth interface and have been produced in the same UHV compatible CVD growth system.

wafers were given an *ex-situ* chemical clean in a Mercury automated spray cleaner, again using a B/CLEAN/R2 clean recipe. To remove the remaining thin surface oxide, the wafers were cleaned with HF prior to the wafers being returned to the growth chamber. Five of the wafers were then subjected to an 880°C oxide desorb (in H_2 at a pressure of 130 Pa) to remove any residual oxide. For one wafer this desorption was carried out at a slightly lower temperature of 800°C.

The heterolayers for the modulation-doping were grown at 605°C at a pressure of 20 Pa. Initially a thin constant composition i-$Si_{0.77}Ge_{0.23}$ buffer was grown with a thickness ranging between 10 nm and 130 nm. The remaining heterolayers were nominally the same in every wafer. On top of a 9 nm thick i-Si quantum well was a 17 nm undoped $Si_{0.77}Ge_{0.23}$ spacer. An 87 nm n-type $Si_{0.77}Ge_{0.23}$ layer

Wafer	Virtual Substrate Ge grading	VS / active layers Ge content	Oxide Desorb Temp. (°C)	Buffer Thickness (nm)
7B22	0-23%	match	880	128
7B23	0-23%	match	880	50
7B24	0-23%	match	880	10
7B25	0-23%	match	800	10
7B26	0-25%	mismatch	880	50
7B27	0-25%	mismatch	880	10

Table 4.1: A summary of the differences in the DERA 7B22-7B27 2DEG series

(uniform dopant concentration $\sim 5 \times 10^{18}$ cm^{-3}) was formed as before. Finally the wafers were capped with a nominal 4 nm Si layer. A summary of the different wafers is presented in table 4.1.

The structures used were optimised for low temperature electrical properties and the design and growth parameters in the material have also been discussed in [139]. Initial regrowth results along with the effect of mismatched Ge concentrations in the virtual substrate and heterolayers were presented in [127]. Samples from the centre of each wafer were processed as described in Section 3.3 and annealed Au (1% Sb)/NiCr/ Au (1%Sb) metal was used for the n-type ohmic contacts.

4.4.4 Results from the 7B Wafer Series

Magnetotransport Results for Measurements at 1.5 K

Magnetotransport results for measurements in the dark at 1.5 K are presented in Table 4.2. The first four wafers in the table, 7B22-25, which have a matched Ge virtual substrate (series A in Figure 4.7), show a decline in carrier density as the buffer layer thickness is reduced. This supports the idea that the regrowth interface contains electron traps. As the regrowth interface approaches the quantum well, it becomes easier for electrons to be excited out of the well and to become trapped at the regrowth interface. A greatly reduced mobility with the thinnest buffers would also suggest that there are of scattering centres present, which is consistent with some form of charged traps.

TEM images of samples from these wafers (Figure 4.10) show a Si rich layer at the regrowth interface and this will have a lower conduction band than the

Wafer Name	Buffer Thickness (nm)	μ cm^{2}V^{-1}s^{-1}	n_s x10^{11} cm^{-2}	R_{Sheet} Ω/square	L_e x10^{-6}m
7B22	128	260 000	3.58	80	2.65
7B23	50	145 000	3.28	140	1.42
7B24	10	123 000	3.01	169	1.15
7B25	10	160 000	3.30	118	1.57
7B26	50	111 000	3.41	165	1.11
7B27	10	64 000	2.73	358	0.57

Table 4.2: A summary of magnetotransport results from the DERA 7B 2DEG series. These measurements have been taken in the dark at 1.5K

bulk $Si_{0.77}Ge_{0.23}$, which could explain the presence of electron traps. Other mechanisms may also account for the traps such as interface roughness, dopant contamination or non-complete oxide removal.

There has been detailed analysis on wafer 7B22 at lower temperatures and higher fields (see [58, 140, 141]). Figure 4.8 shows the longitudinal and Hall magnetoresistivity at 50 mK for sample 7B22. This plot was taken by N. Griffin and R. B. Dunford has been reproduced from [141]. It shows strong SdH which start around 0.2 T. These undergo first spin- and then valley-splitting as the field is increased, and at higher fields, there are clear zeros at integer filling factors, which are accompanied by quantum Hall plateaux. At filling factors between 1 and 2, additional structure due to the fractional quantum Hall effect is observed. The data shows strong ρ_{xx} minimum at $\nu = \frac{4}{3}$, and it has been suggested that this may correspond to $\nu = \frac{2}{3}$ in both valleys. The absence of clear field or temperature dependence close to B = 0 T indicates that effects due to interactions, weak-localisation and screening are small.

Dingle plots were used to find the quantum lifetime, ($\tau_q = 4.9$ ps) and the lifetime ratio ($\alpha = 8.1$). The large α values indicate a dominance of small-angle scattering. This is most likely due to the remote ionised impurities in the doping layer. More details on this and other unusual features of the magnetoresistance data, such as Hall overshoots can be found in [58, 140, 141].

In the GaAs/AlGaAs system [142] 2DEGs grown with buffers of 200 nm thickness or greater were found to have no degradation in mobility or carrier density from conventionally grown 2DEGs in the MBE system. For a 110 nm buffer the carrier density was reduced. The mobility was reduced to 42% of a conventional

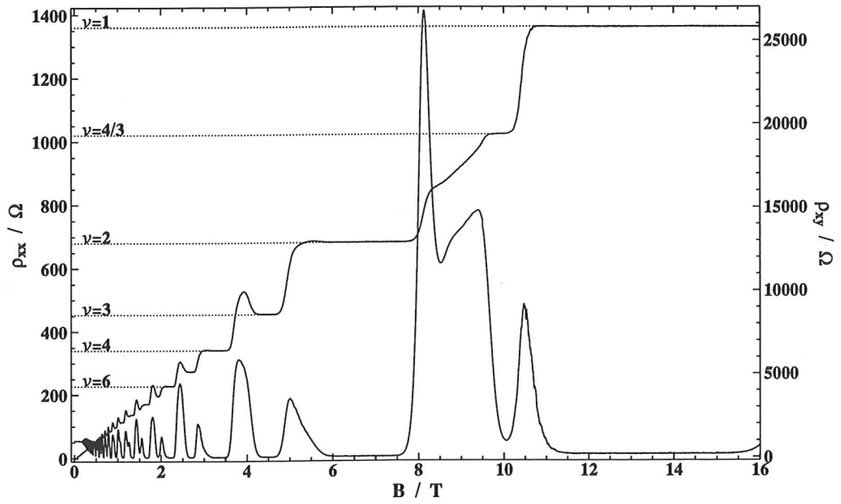

Figure 4.8: Magnetotransport measurements taken in perpendicular magnetic fields up to 16 T, for samples from DERA Si/SiGe 2DEGs wafer 7B22 at 50 mK. Well-defined Shubnikov-de Haas oscillations and both integer and fractional quantum Hall effect plateaux can be seen.

2DEG growth without a regrowth interface. For a 60 nm buffer, the mobility was reduced to 32% of the conventional 2DEG growth. In the present SiGe system using the low temperature oxide desorb with a 10 nm buffer, the mobility was reduced to 62% of a conventional 2DEG growth, substantially better than the GaAs/AlGaAs results. In addition, no degradation in mobility was found in samples with buffers down to 128 nm.

The sample with the 128 nm buffer, 7B22, actually has a higher mobility than comparable samples without a regrowth interface and has the highest mobility to date for a Si/SiGe 2DEG with a regrowth interface. This wafer was the first of the 7B series to be grown after more than 25 μm of undoped material had been grown in the CVD system. This is substantially more than normal and reports from DERA indicate that it left an usually low background contamination of dopants (much lower than the other 7B series wafers), however the electrical behaviour is still dominated by unintentional impurities. The magnetoresistance results are similar to results from higher mobility samples [18] and this demonstrates that the regrowth interface in this sample has little effect on the quantum transport.

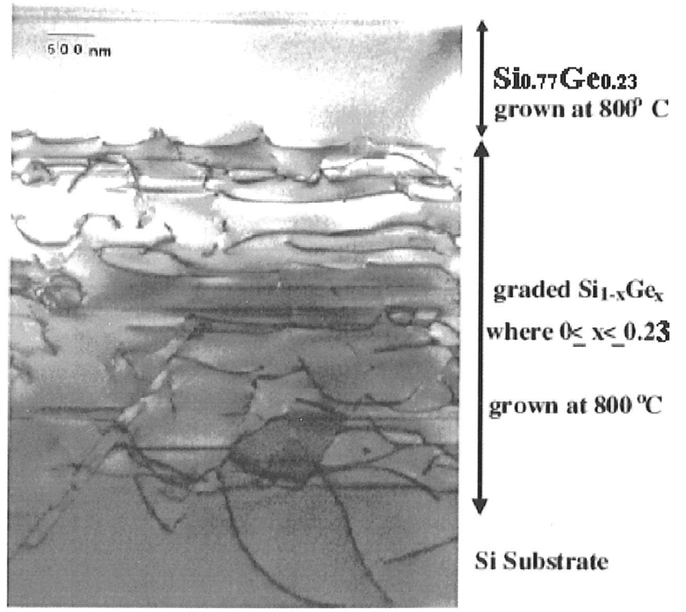

Figure 4.9: TEM image of DERA Si/SiGe 2DEG wafer 7B22

TEM Images and Oxide Desorb Temperatures

Figure 4.9 is a cross-sectional TEM of wafer 7B22. This structure shows the threading dislocations in the virtual substrate as dark lines. It can be seen that although there is a high volume of dislocations in the graded region, none are visible in the upper layers near the surface. This shows that only a few dislocations penetrate through to the surface and so the chance of seeing a dislocation in the upper region of the structure is very low in any one cross-sectional slice. The low background impurity density together with the large buffer that helps to keep the threading dislocations away from the 2DEG results in a very high mobility.

Wafers 7B24 and 7B25 have structures that nominally identical, however 7B25 has an 800°C oxide desorb whereas 7B24 is similar to the 6B wafers and the rest of the 7B series in that it has an 880°C desorb. Figure 4.10a shows a cross-sectional TEM through a sample from wafer 7B24 with the 880°C thermal desorption and Figure 4.10b shows a cross-sectional TEM through a sample from wafer 7B25 with an 800°C desorb.

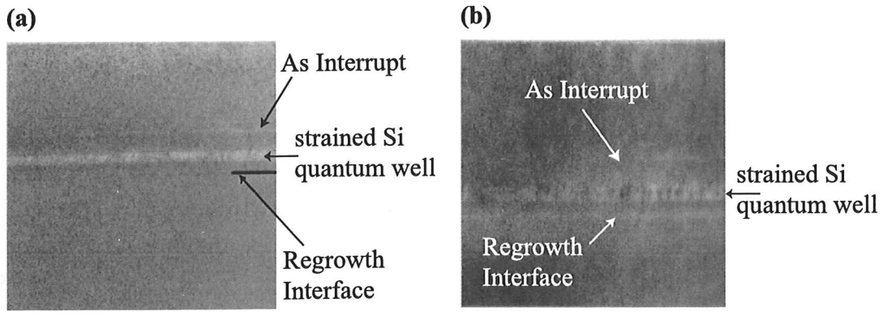

Figure 4.10: (a) TEM of wafer 7B24, which has an 880°C thermal oxide desorb. (b) TEM of wafer 7B25, which has an 800°C thermal oxide desorb.

The Si quantum wells are clearly visible as a stripe of bright contrast approximately 100 nm below the surface of the layers. 10 nm below the Si channels, the position of the cleaned growth interfaces can be observed as a thin line running parallel to the Si well. It is thought that the contrast at these interfaces is due to a thin Si rich layer, which occurs either from the cleaning or during the initial stages of regrowth. The onset of As doping also gives a similar contrast just above the quantum well.

The Si-enriched region at the regrowth interface will have a lower conduction band than the bulk SiGe, which may result in the presence of electron traps at the interface. An increase in surface roughness and the possibility of a greater density of electron traps in the wafer with the higher desorb temperature, should result in wafer 7B24 having inferior transport properties when compared to wafer 7B25. This agrees with the results given in Table 4.2, which indicates that the lower temperature desorb has a higher n_s and an improved mobility. The lower temperature oxide desorb seems to have lowered the electron trap density at the regrowth interface. The lower temperature oxide desorb is possibly more efficient at removing the residual oxide but further investigations are required to determine the mechanisms behind the increase in mobility and carrier density with reduced thermal budget cleaning.

4.4.5 Comparison of Wafers with Matched Ge/ Mismatched Ge Virtual Substrates

Three of the wafers used in this study on the effects of the regrowth interface (6B121, 7B26 and 7B27), have a virtual substrate that has been linearly graded in Ge from 0% to 25% followed by a step down to 23% in the constant buffer region of the virtual substrate. The wafers have a 2% mismatch in the Ge concentration between the graded region and the constant composition buffer region in the virtual substrate. The other four wafers (7B22 - 7B25) do not have this mismatch and have been graded from 0% to 23%, followed by a thick $Si_{0.77}Ge_{0.23}$ constant composition virtual substrate.

This permits an investigation into whether a stepped buffer (with a Ge mismatch) has a beneficial or detrimental effect on the electronic properties. It was believed that a mismatched Ge composition would lead to a greater level of strain relaxation through the graded layers and hence give improved carrier mobilities [37].

The mobility and carrier density of the matched and mismatched Ge samples have been plotted in order to see more clearly the effect of the mismatch on the electronic properties. Figure 4.11 shows two graphs, one of which shows the mobility of samples from wafers with matched Ge and mismatched Ge virtual substrates and the other shows the different carrier densities. All of samples that are shown in Figure 4.11 have been oxide desorbed at the same temperature of 880°C. The 128 nm Ge mismatched virtual substrate sample, is from wafer 6B121 and has been included for comparative purposes.

Figure 4.11 shows that samples with a matched lattice have a substantially higher mobility regardless of the buffer thickness. The difference in sample mobility increases with buffer thickness, but it should be noted that the 128 nm sample with a matched Ge composition, has produced after more than 25 μm of undoped material had been grown in the CVD system and so has a very large mobility since there is a lower background impurity density.

There is a similar trend with the carrier density, however when comparing the carrier densities of samples with a 50 nm spacer, the sample with a mismatched interface has a carrier density that is slightly larger than the sample with a matched interface. This seems to be an anomalous result and is not consistent with the other results presented here.

The reduction in mobility is more pronounced in the thinner buffer samples

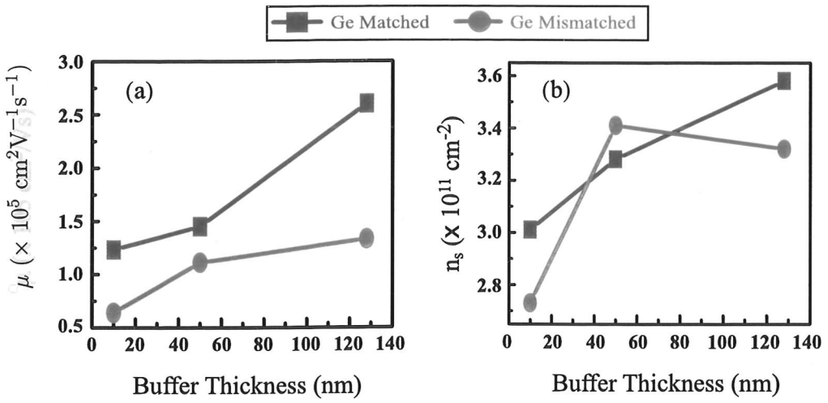

Figure 4.11: The mobility (μ) and carrier density (n_s) for Ge matched and mismatched virtual substrates.

and for the 10 nm buffers the mismatch reduces the mobility by a factor of 2. It is difficult to explain this in terms of scattering since this should not be affected by the mismatch.

The reduction in mobility can be accounted for by strain since the equilibrium critical thickness for a 2% Ge mismatch is about 800 nm [23], the Ge mismatched wafers suffer from increased strain. Hence the reduction in mobility may be due to increased strain and not relaxation of the heterolayers. The reduction in the conduction band discontinuity that the quantum well experiences due to the strained SiGe [49] is consistent with the reduction in the carrier density in the quantum well.

Mobility vs. 2D Sheet Carrier Density Plot

Figure 4.12 shows a plot of mobility against 2D sheet carrier density at a temperature of 1.5 K, for results from the 6B and 7B series. Data from 7 other DERA wafers (all of which have been grown in the same UHV compatible CVD system) have also been plotted (data taken from [127, 58, 143, 126]). The 6B and 7B series are shown as open squares. The dots, which are for samples taken from across wafer 7B25, show the uniformity and these are discussed in detail in chapter five. The solid squares are for samples from wafer 7B22, which has a substantially lower background impurity density than the other wafers [127, 141, 58, 126]. Two theoretical curves from Stern and Laux [137] are plotted for comparison, b[illegible]th of

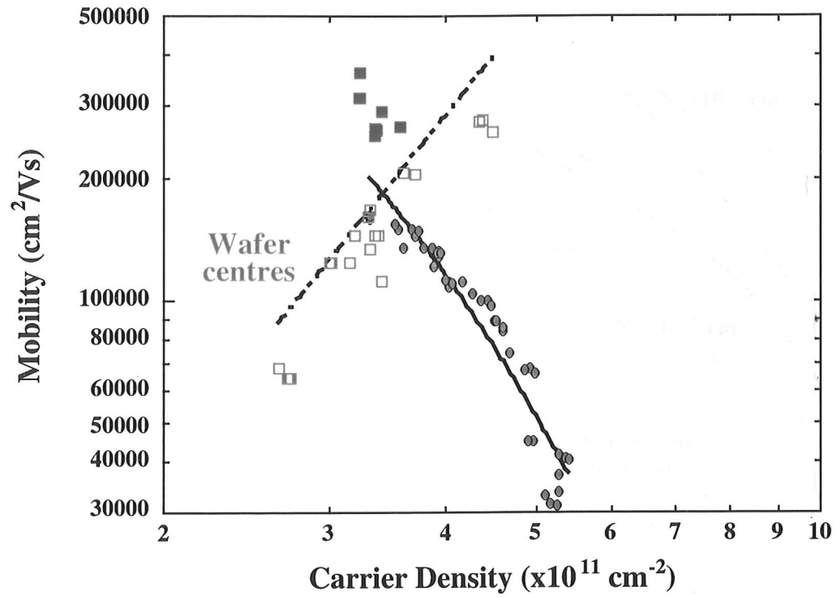

Figure 4.12: The Hall mobility (μ) as a function of carrier density (n_s), temperature of 1.5 K, for results from the 6B and 7B series. Data from 7 other DERA wafers are also shown (data taken from [127, 58, 143, 126]). The 6B and 7B series are shown as open squares. The red dots are taken from across wafer 7B25 and show the uniformity (discussed in chapter five). The solid squares are for samples from wafer 7B22, which has a substantially lower background impurity density than the other wafers [127, 141, 58, 126]. Two theoretical curves from Stern and Laux [137] are plotted for comparison.

Figure 4.12 shows that the mobility is independent of substrate Ge concentration, oxide desorb temperature, spacer thickness and buffer layer thickness after cleaning.

An initial investigation into the mobility-carrier density relationship for the 6B and 7B series samples, gave a $\mu = \alpha + \beta n^{1/2}$ scaling where α and β are constants (α represents quantum corrections from weak localisation and electron-electron interactions) [126,127]. The $\mu = \alpha + \beta n^{1/2}$ behaviour had been reported before [139] in similar tensile strained Si modulation-doped 2DEGs, where the mobility is limited by background impurity scattering. Using the theory of Gold [144], a background impurity density (N_B) of 1.1×10^{15} cm^{-3} was extracted from the

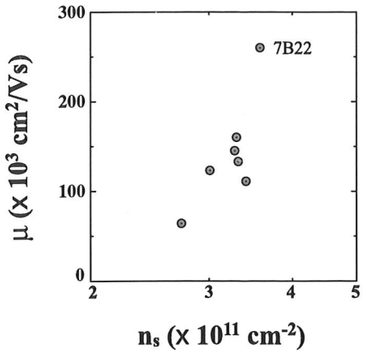

Figure 4.13: The Hall mobility (μ) as a function of carrier density (n_s), temperature of 1.5 K, for results from the 6B and 7B series only.

data, consistent with other measurements of the background density in the growth chamber [139].

However an analysis of the data by Crow and Abrahams [145] suggests that the mobility follows a $\mu = \beta n^{\gamma}$ relationship. Their model suggest that the power law decrease in mobility is the combination of interface roughness scattering and remote ionised impurity scattering.

The explanation for the lower mobilities with the thinner buffers is partially due to a reduction in the carrier density, associated with electron traps at the regrowth interface. However, the effects of increased scattering from other mechanisms such as the regrowth interface cannot be neglected at present and further research is required to obtain a full understanding.

Figure 4.13 shows a plot of mobility against 2D sheet carrier density at a temperature of 1.5 K, for results from the 6B and 7B series only. The single sample grown with the reduced background (7B22) does not lie with the rest of the 7B and 6B series, suggesting that higher low-temperature mobilities are possible for appropriately designed and grown samples in the present CVD system.

4.5 Conclusions

The chapter presents results from modulation-doped 2DHG and 2DEG structures that have been grown by UHV compatible CVD on SiGe virtual substrates. Results from samples with conventional 2DHG and 2DEG structures have been presented in Section 4.2 and Section 4.3. This chapter also explores the production of modulation-doped 2DEGs structures that include a regrowth interface.

A two stage growth process has been used to provide wafers with a regrowth interface. After the initial growth of a virtual substrate wafers are removed from the growth chamber. They are chemically cleaned before being returned to the CVD system. The remaining modulation-doped 2DEG heterolayers are grown as normal. It has been shown that it is possible to incorporate a regrowth layer in Si/SiGe structures without significantly affecting the performance of fabricated devices.

Comparing samples with a regrowth interface to ones grown in a single step process shows that the inclusion of a regrowth interface has an adverse effect on the transport properties, with a reduction in both the Hall mobility and carrier density. The best results indicate that the mobility is reduced to 62% of a conventionally grown 2DEG for a 10 nm buffer layer, significantly better than comparable experiments in the GaAs/AlGaAs system.

Scattering from the cleaned interface as well as increased interface roughness will account for this reduction but it is important to note that the Si rich interface itself will have a number of electron traps. As the buffer thickness between the interface and quantum well is reduced, it becomes easier for the electrons to be excited out of the quantum well and to become trapped at the regrowth interface, thus accounting for the carrier density and mobility decrease.

Three of the wafers used in this study have a 2% mismatch in the Ge concentration between the graded region and the constant composition buffer region in the virtual substrate. The other four wafers do have this mismatch and have been linearly graded from 0% Ge to 23% Ge, followed by a thick $Si_{0.77}Ge_{0.23}$ constant composition virtual substrate. It has been shown that a stepped buffer (with a Ge mismatch) has a detrimental effect on the electronic properties. The increased strain, caused by the mismatch, leads to a reduction in the carrier density as well as causing a decrease in Hall mobility.

Lower temperature desorption of the passivating chemical oxide (produced by the FSI clean) improves the mobility and carrier density, when a regrowth interface is close to the quantum well. A comparison of two wafers, 7B24 and 7B25 show that the lower temperature oxide desorb may be responsible for reducing the electron trap density at the regrowth interface thus improving the material properties. The lower temperature desorb may be more efficient at removing any residual oxide and lower temperature processing could be responsible for a decrease in surface roughness. Section 4.4 explores some of the basic technological stages required in producing complicated multi-epitaxial step devices [127,146]

which may be required if selective SiGe MODFET growth is to be produced on a chip, as may be envisaged for certain types of integration. The successful incorporation of a regrowth layer within high quality working 2DEG devices demonstrates the possibility of treating a virtual substrate as any other substrate and that *ex-situ* treatment and *ex-situ* processing is possible. The technique of regrowth potentially offers flexible fabrication technology in the Si/SiGe system.

Chapter 5

Wafer Uniformity

5.1 Introduction

This chapter examines the effect of non-uniformity in material properties across a wafer. Due to limitations in the amount of material available detailed analysis has been carried out a typical wafer grown by DERA. All of the Si/SiGe wafers that have been received from DERA have been grown in the same UHV compatible CVD growth chamber and it is reasonable to assume that wafers from the same system will have similar uniformity/non-uniformity characteristics. Chapter four shows that it is possible to incorporate a regrowth step in Si/SiGe wafer growth and still produce working devices. This chapter focuses on samples from DERA wafer 7B25, which contains a regrowth interface, described in the preceding chapter.

A limitation of the UHV compatible CVD system used to grow 7B25, is the presence of a radial thermal gradient across the substrate during growth. One important consequence is that the edge of the wafer is slightly cooler than the centre, resulting in a different growth rate for Si across the wafer. This variation in growth rate can cause a significant non-uniformity in wafer structure.

Any degree of non-uniformity, may be utilised for research purposes. Samples from the same wafer will have a very similar background impurity concentration and will have been subjected to the same growth conditions. Any variation in transport properties of samples taken from across a wafer, should therefore be due to any differences in wafer structure. This makes it possible to study the transport properties as a function of Ge fraction, dopant concentration and layer thicknesses.

The predicted variation in the growth temperature of the substrate across the wafer is shown in Figure 5.1 using data received directly from DERA. During the wafer growth the measured temperature at the centre of the wafer is 606°C whilst the edge of the wafer, the growth temperature is around 588°C. While the thermal gradient prevents the use of the present system for manufacture, it allows the investigation of electronic properties as a function of different growth parameters within a single wafer.

Magnetotransport properties of samples from each wafer will be used to assess the wafer uniformity and quality. Samples taken at regular intervals from each wafer have been processed simultaneously in order to limit any variation due to the device fabrication process. Hence any variation in electronic properties across a wafer should result from differences in material quality only.

Results from electrical assessment at 1.5 K will be provided in Section 5.3. Other structural measurement techniques such as TEM, SIMS and AFM have been used whenever possible and results from these are presented in Section 5.4. An analysis of all of the results from DERA wafer 7B25 is presented in Section 5.5. Results from this section are presented in [147].

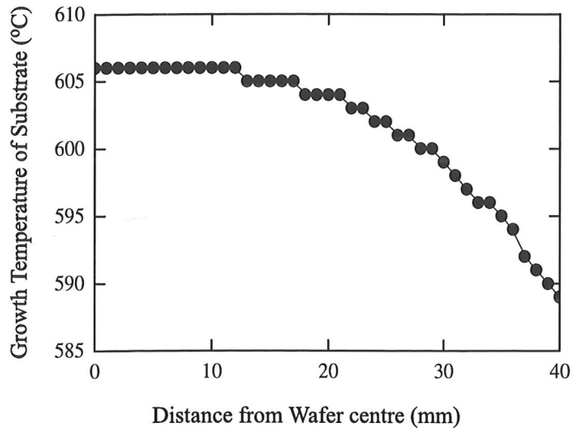

Figure 5.1: The growth temperature of the wafer substrate as a function of the distance from the wafer centre, for wafers produced in the DERA UHV compatible CVD growth system. Data provided by DERA.

5.2 Wafer Structure for DERA7B25

The nominal structure of wafer 7B25 is shown in detail in figure 5.2. On the p-Si(100), 100 mm substrate there is a 4 μm thick linearly graded $Si_{1-x}Ge_x$ alloy ($0\% < x < 23\%$) followed by a 1 μm thick i-$Si_{0.77}Ge_{0.23}$ constant composition buffer. At this point there is a regrowth interface caused by an *ex-situ* chemical clean. Wafer 7B25 is was given an 800°C oxide desorb in H_2 at a pressure of 130 Pa, when it was returned to the growth chamber.

A 10 nm i-$Si_{0.77}Ge_{0.23}$ buffer approximately 10 nm thick, separates the regrowth interface from the strained undoped Si channel, which has been designed to be 10 nm thick. Above this there is an undoped $Si_{0.77}Ge_{0.23}$ spacer, nominally 17 nm thick, followed by an 87 nm n-$Si_{0.77}Ge_{0.23}$ As doped region. The wafer is capped with a nominal 4 nm thick Si layer. The design and growth parameters have been discussed in detail in Section 4.4 and also in [139, 143].

A strip of material running from the centre of the wafer to the edge was removed for processing. Samples, 2 mm apart, have been taken from across the wafer and have been processed as described in Section 3.3. Annealed Au (1% Sb)/NiCr/Au(1% Sb) metal was used for the n-type ohmic contacts.

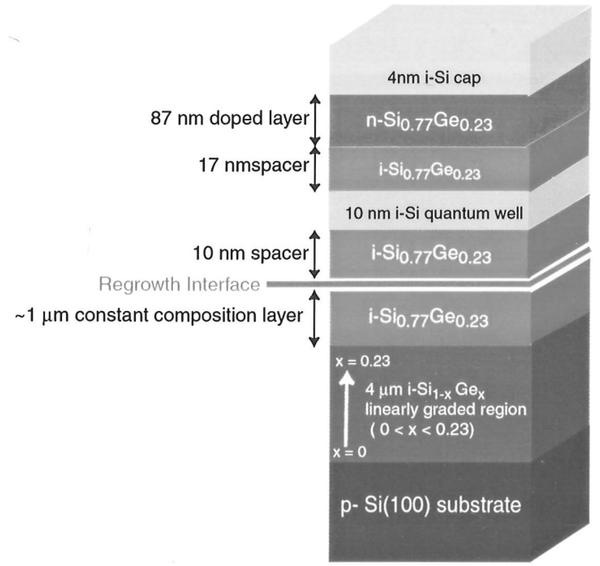

Figure 5.2: The designed structure of DERA wafer 7B25.

5.3 Results of Electrical Characterisation

All samples displayed Shubnikov-de Haas oscillations when tested at 1.5 K in the dark and have Hall mobilities of up to 161 000 $cm^2V^{-1}s^{-1}$ at a carrier concentration of 3.5×10^{11} cm^{-2}. Typical Shubnikov de Haas oscillations and Hall measurements are shown in figure 5.3 for samples from the centre and edge of the same wafer. The centre sample is 4 mm from the wafer centre and shows a Hall mobility of 161 000 $cm^2V^{-1}s^{-1}$ for a carrier concentration of 3.53×10^{11} cm^{-2}. The sample from the edge of the wafer is 40 mm from the wafer centre (10 mm from the edge) and shows a significantly lower Hall mobility of 43 500 $cm^2V^{-1}s^{-1}$ for a much larger carrier concentration of 5.4×10^{11} cm^{-2}. An examination of the higher mobility sample shows that both spin and valley splitting are resolved even at low magnetic fields and at 1.5 K.

The magnetotransport results from the samples that were tested show a clear monotonic variation in the Hall mobility and carrier density across the wafer. To see this variance more clearly, the mobilities and carrier concentrations have both been plotted against the distance from the wafer centre in figure 5.4. The carrier concentration is seen to increase whilst there is a decrease in mobility going from the centre of the wafer to the edge of the wafer. The non-uniformity in the carrier density can be attributed to differences in the structure at the centre and edge (further discussed in Section 5.4.2).

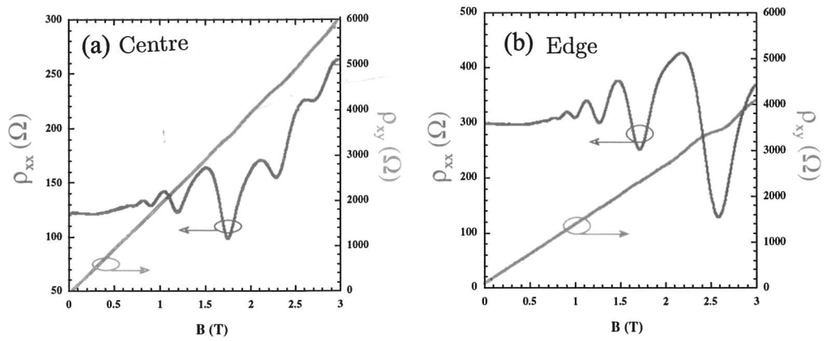

Figure 5.3: Shubnikov-de Haas oscillations and Hall plateaux for samples from 7B25. These measurements were taken in the dark at 1.5 K. The SdH oscillations and the Hall gradient are shown for sample (a) 4 mm from the wafer centre (with a mobility of 161 000 $cm^2V^{-1}s^{-1}$ for a carrier density of 3.2×10^{11} cm^{-2}) and sample (b) 40 mm from the wafer centre (with a mobility of 43 500 $cm^2V^{-1}s^{-1}$ for a carrier density is 4.8×10^{11} cm^{-2}).

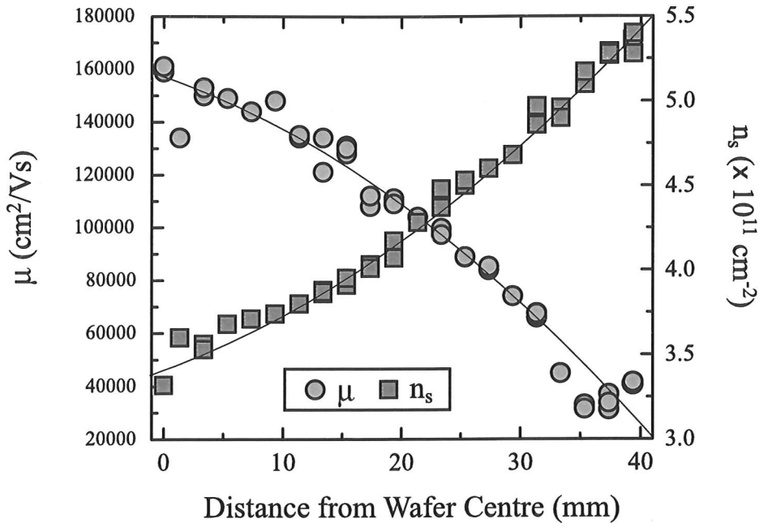

Figure 5.4: Mobilities and carrier concentrations from samples 2mm apart, from wafer 7B25, plotted against the distance from the wafer centre. The mobility is shown as the circles and the carrier density has been plotted as the squares. The solid lines are guides to the eye.

As the number of electrons in the well increases there is an associated increase in electron screening of the dopants in the dopant supply layers and this should help to increase the mobility. There is also an associated increase in inter-electron scattering which will have a negative effect on the mobility, however this will only have a significant effect at significantly larger carrier densities than those displayed by the current samples. The observed decrease in mobility can be explained by variation in the wafer structure and is discussed in detail in Sections 5.4 and 5.5.

In the CVD growth system used to produce wafer 7B25, the mobility of 2DEGs has been shown to depend strongly on the carrier density in the system (as shown in chapter four) and so electron scattering parameters, such as the mean free path (l), may be more informative. The mean free path is the average distance that the electron is able to travel before it is scattered and can be expressed as:

$$l = \frac{\mu\hbar}{e}(n_s\pi)^{\frac{1}{2}} \tag{5.1}$$

where μ is the Hall mobility and n_s is the carrier concentration.

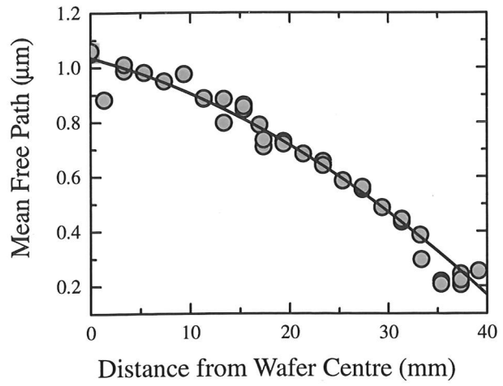

Figure 5.5: The mean free path, l, versus distance from the wafer centre for DERA wafer 7B25. The fitted curve is a guide to the eye.

Figure 5.5 shows the change in the electron mean free path across the wafer. It is apparent that the mean free path of the electrons decreases significantly towards the edge of the wafer. This indicates that towards the edge of the wafer, there is an increase in scattering. This can be attributed to several different scattering mechanisms such as increased remote ionised impurity scattering as well as increased interface roughness scattering. The regrowth interface present in the 7B25 structure also has a significant effect on the electronic properties and the role of the these various scattering mechanisms is discussed in detail later in Section 5.5.

5.3.1 Quantum Lifetime Measurements for Samples from Wafer 7B25

For the two samples, taken from different parts of the same wafer, shown in Figure 5.3, the electron transport lifetime, τ_t, and the quantum lifetime, τ_q, have been found. These have been used to calculate $\alpha = \frac{\tau_t}{\tau_q}$, the scattering lifetime ratio and all of these are presented in Table 5.1. The quantum lifetimes and scattering lifetime ratio have been defined in Section 2.7.

Table 5.1 shows that there is a large difference in the transport lifetime with $\tau_t = 18.0$ ps near the wafer centre and $\tau_t = 4.77$ ps, near the wafer edge. There is a noticeable difference in α, with $\alpha = 8.44$ for samples 4 mm from the wafer centre, whereas at 40 mm from the wafer centre it is a much lower value of $\alpha = 2.58$. In comparison there is a much smaller change in the quantum lifetime,

Distance of sample from wafer centre (mm)	τ_t, Transport Lifetime (ps)	τ_q, Quantum Lifetime (ps)	α ($\alpha=\tau_t/\tau_q$)
4	18.0	2.13	8.44
40	4.77	1.85	2.58

Table 5.1: Scattering lifetimes for samples from the centre and edge of wafer 7B25

with $\tau_q = 2.13$ ps near the centre of the wafer and $\tau_q = 1.85$ ps, near the edge of the wafer.

It has been shown that when $\alpha = 1$ short-range interface roughness scattering dominates and for $\alpha \gg 1$,small angle, long range, remote ion scattering dominates (as in Ga/AlGaAs heterostructures) [148]. In lower mobility samples (where the scattering may arise from short range potentials caused by impurities closer to the channel), the difference between the two scattering times is expected to be minimal and any scattering is expected to be independent of the angle of scattering. Near the edge of the wafer, the mobility is much lower and the dopant layer is much closer to the quantum well and results presented in Table 5.1 show that there is a smaller α for samples from the wafer edge.

In high mobility modulation-doped heterostructures the mobility can be limited by scattering from remote ionised impurities in the dopant layer. The disorder potential from these is long range in nature, so there is a predominance of small angle scattering and the transport lifetime, τ_t, is expected to be much larger than τ_q [82]. The electrons are confined to a plane parallel to the doping layer and as the distance between regions increases, α increases (*i.e.* τ_t will increase more rapidly than τ_q). This is shown to be the case here, with α increasing towards the wafer centre, where the better mobility samples have a larger spacer thickness (see Section 5.4).

The ratio α has values that range between 2.58 and 8.44 for the samples that have been measured here. This is consistent with results from other similarly grown wafers that have been produced in this system [141]. Theoretical calculations have been carried out on structures that are similar in composition to the ones that have been used here. Calculations by Stern and Laux [137] have shown that $Si/Si_{0.7}Ge_{0.3}$ heterostructures with spacers of 5 nm to 12 nm require $\alpha = 10$ - 20 for remote ionised impurity scattering to limit the mobility. For strained $Si/Si_{1-x}Ge_x$ heterostructures where $0.21 < x < 0.23$, calculations suggest that the combination of remote ionised impurities and surface roughness scat-

tering are the important scattering mechanisms in the low-field low-temperature limit (see work by Crow and Abram [145]).

The results obtained in this study agree with these theoretical calculations and illustrate the significance of interface roughness scattering and remote ionised impurity scattering. There are other factors such as the effect of the regrowth interface, which have not been discussed in detail in theoretical papers, but which may also be important for the present system.

5.4 Non-Electrical Measurement Techniques

As well as low temperature electrical characterisation, other techniques such as Secondary Ion Mass Spectrometry (SIMS), Transmission Electron Microscopy (TEM) and Atomic Force Microscopy (AFM) have been used to assess wafer quality at the centre and edge of the wafer. AFM was used to investigate the surface morphology of both wafers [104]. A Digital Instruments Dimension 3000 AFM [123] was used to obtain images of the centre and edge of wafer 7B25.

5.4.1 Secondary Ion Mass Spectrometry

SIMS has been used to obtain an accurate depth profile of the dopant densities and Ge content across the sample. Figure 5.6 is a SIMS profile of samples from the centre of wafer 7B25, whereas Figure 5.7 is a SIMS profile of samples from the wafer edge.

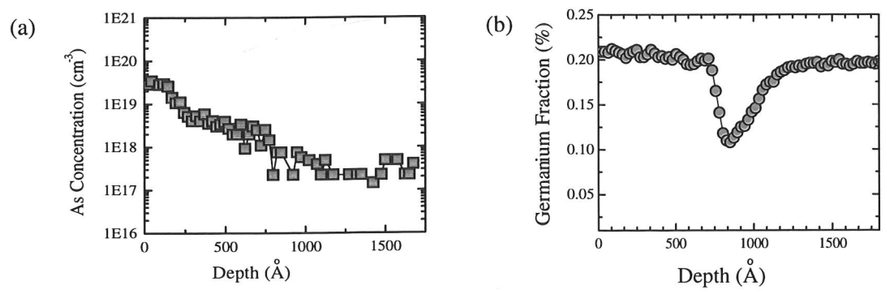

Figure 5.6: SIMS data from the centre of DERA wafer 7B25. (a) shows the As concentration as a function of the depth in the wafer. The dopant profile has a resolution limit in the low 10^{17} cm^{-3} range. (b) shows the Ge fraction within the wafer. The Si quantum well is not fully resolved in the Ge profile.

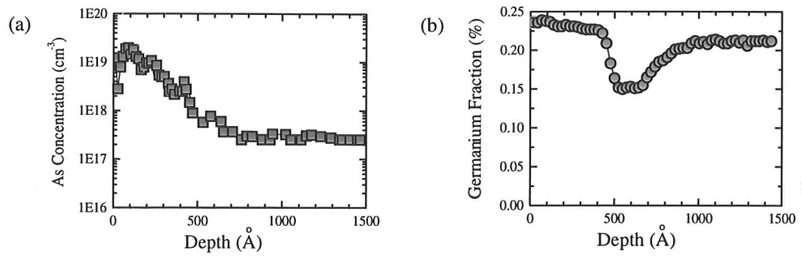

Figure 5.7: SIMS data from the edge of DERA wafer 7B25. (a) shows the As concentration as a function of the depth in the wafer. The dopant profile has a resolution limit in the low 10^{17} cm^{-3} range. (b) shows the Ge fraction within the wafer. The Si quantum well is not fully resolved in the Ge profile.

The dopant profiles obtained from the SIMS data reveal that the As concentration is uniform across the wafer (within experimental limits of accuracy). There is an obvious difference in the Ge concentration across the wafer resulting in a bulk composition of $Si_{0.79}Ge_{0.21}$ close to the wafer centre, whereas near the edge of the wafer the bulk composition is $Si_{0.77}Ge_{0.23}$. The larger Ge fraction at the edge of the wafer means that there is a deeper quantum well at the edge than at the centre. It should be noted that SIMS depth resolution does not fully resolve the strained quantum well.

5.4.2 Transmission Electron Microscopy

TEM can be used to measure the thickness of the grown layers [120]. Figure 5.8 shows two TEM images, one for a sample taken from the wafer centre and the other for a sample near the edge of the wafer. The thick dark band across the centre of the TEM, approximately 100 nm below the surface of the layers, is the strained Si quantum well. The contrast at the interface due to the chemical clean is visible as a lighter stripe about 10 nm below the Si quantum well and is due to a thin Si rich layer that occurs whenever the growth of the $Si_{1-x}Ge_x$ alloy is interrupted. Also marked is the point where As incorporation begins, which shows up as a faint dark line about 15 nm above the band of Si.

The TEM images are shown on the same scale, which allows a direct comparison of the layer thickness between the centre and edge of the wafer. A close examination of TEM images shows that there is a clear change in the thickness of the SiGe buffer, Si quantum well doping supply layer and SiGe spacer across the wafer.

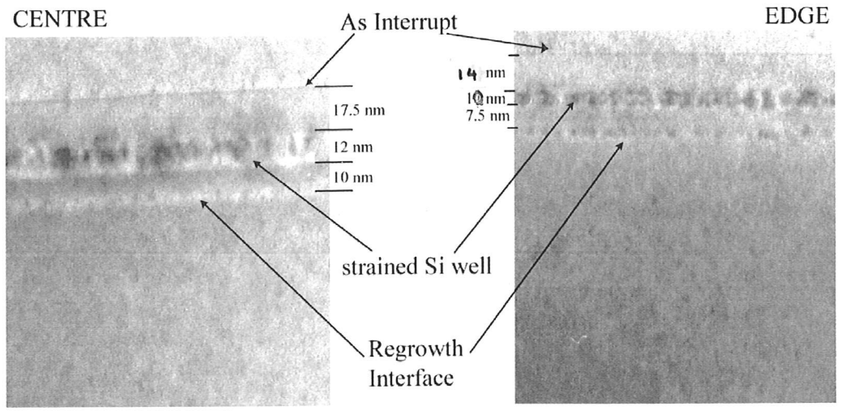

Figure 5.8: TEM images from the centre and edge of DERA wafer 7B25

The TEM images show that whilst the quantum well at the edge of the wafer is at the desired value of 10 nm, it is 12 nm thick near the wafer centre. The Matthews and Blakeslee critical thickness [23] for strained Si is 15.7 nm for a $Si_{0.79}Ge_{0.21}$ virtual substrate and 14.1 nm for a $Si_{0.77}Ge_{0.23}$ virtual substrate. For both the wafer centre and the wafer edge, the quantum well thickness is below the Matthews and Blakeslee critical thickness and hence strain relaxation and defects are unlikely to occur and no defects are observed in the TEM images.

The 17.5 nm spacer thickness at the centre is much larger than the 14 nm spacer thickness at the edge. The TEM images show that at the edge of the wafer the regrowth interface is only 7.5 nm away from the Si quantum well, whereas at the centre it is 10 nm away. TEMs do not give an accurate profile of the top Si layers so it is difficult to gauge the depth of the cap.

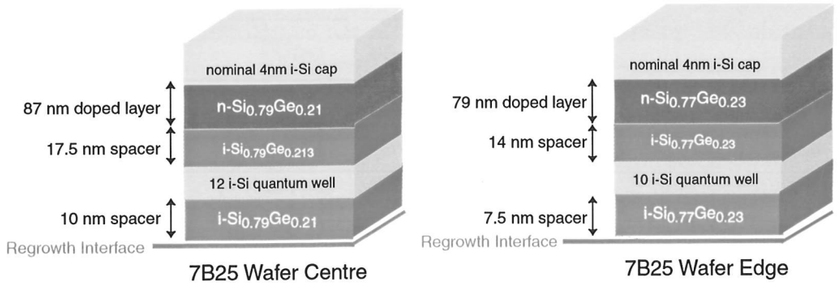

Figure 5.9: The actual structure at the centre and edge of DERA Wafer 7B25. This has been calculated using TEM images and data extracted from SIMS measurements.

These variations in layer thicknesses clearly demonstrate the difference in structure due to the change in growth rate of the wafer with temperature. The difference in the SiGe composition as well as the change in the layer thickness are shown for both the wafer centre and wafer edge in Figure 5.9.

5.4.3 AFM Images

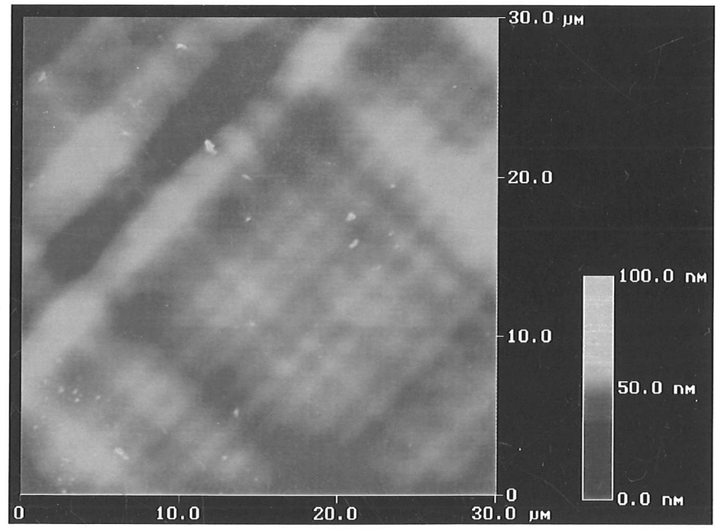

Figure 5.10: AFM image from the centre of DERA Wafer 7B25. The bright to dark contrast is in the vertical direction has a range of 100 nm.

AFM images from 7B25 samples are shown in Figures 5.10 (taken from near the wafer centre) and 5.11 (taken from near the wafer edge). The contrast on the AFM images represents the vertical height of features on the surface and the difference in height between the brightest (highest) and darkest (lowest) parts of all of the images used in this section is 100 nm. This is the maximum value shown on the colour bar of each image. A comparison of Figures 5.10 and 5.11 shows that surfaces are qualitatively similar and exhibit the familiar cross-hatch pattern that is caused by the Ge grading in the virtual substrate.

As mentioned in chapter one, the characteristic cross-hatch pattern along the <110> direction corresponds to the intersection of the {111} dislocation-glide planes with the (100) surface and their initial formation may result from atomic steps due to dislocation glide [43] and from the inhomogeneous strain field caused

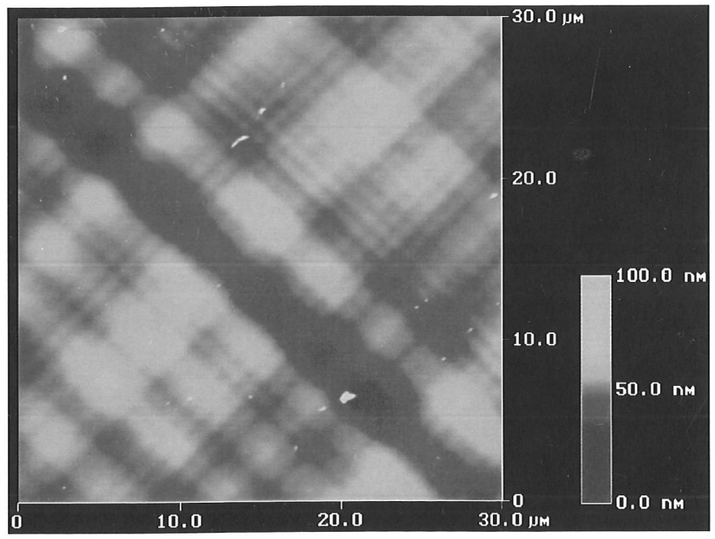

Figure 5.11: AFM image from the edge of DERA Wafer 7B25. The bright to dark contrast is in the vertical direction has a range of 100 nm.

by underlying misfit segments [44]. The periodicity of the cross-hatch patterns is only a few μm at the centre and the edge. These images can be use to extract information about the surface morphology such as the root mean square (rms) height, the mean roughness and the lateral heights (Z range). Data extracted from centre and edge samples from both wafers are presented in Table 5.2.

Figures 5.10 and 5.11 shows that the centre image is slightly more uniform in its contrast and this is reflected by the results in Table 5.2, which show that the centre has a lower mean square height and mean roughness values than the edge. Samples from the edge of the wafer show a greater range of lateral heights and the increased roughness near the edge of the wafer is probably related to the increased Ge content.

Surface Roughness	7B25 Centre	7B25 Edge
Root Mean Square height (nm)	3.69	5.36
Lateral height (nm)	71.2	126
Mean roughness (nm)	2.81	4.10

Table 5.2: The surface roughness as measured by AFM for DERA wafer 7B25.

5.5 Discussion of Results

Chapter four shows that as the regrowth interface gets closer to the quantum well, there is a reduced mobility from the increased scattering. TEM images presented in Section 5.4.2 show that at the edge of wafer 7B25, the regrowth interface is only 7.5 nm away from the quantum well and slightly closer than at the centre of the wafer, where it is 10 nm from the Si well.

Samples that have a regrowth interface still display carrier densities that are 90% of the values obtained by samples without any interface. The increased proximity of the interface to the well at the wafer edge should have a more pronounced effect on the mobility, which falls substantially more than the carrier density.

The TEM images show that there is a narrower spacer between the doped region and the Si well at the edge of the wafer than at the centre. The SIMS profiles of samples from the wafer centre and the wafer edge (Figures 5.6 and 5.7), show that there is a uniform As concentration across the wafer. Since the dopant concentration is approximately constant across the wafer and there is a reduced buffer thickness between the doped region and the quantum well at the wafer edge, this will increase the carrier density at the wafer edge. However the reduced spacer thickness will lead to an increase in ionised impurity scattering from the remote supply layer which will have a detrimental effect on the Hall mobility.

The SIMS profiles shows that there seems to be a difference in the Ge concentration across the wafer (Figures 5.6 and 5.7). A larger Ge fraction at the edge of the wafer means that there is a larger conduction band offset and hence a deeper quantum well, which would explain the increase in the carrier density at the wafer edge. In other work carried out on material grown in the same system under similar conditions, samples which have a larger Ge fraction ($0.27 < x < 0.31$) with similarly sized quantum wells, display a lower Hall mobility and carrier concentration for electrical transport measurements carried out at 1.5 K to 1.7 K [139, 136].

Figure 5.9 clearly shows that the quantum well varies in thickness across the wafer. Ordinarily a reduction in the quantum well thickness would result in a lower carrier density due to the extra confinement in the well pushing the occupied sub-bands up in energy. The wells in the present system are too wide for this to be a significant effect and hence this is negated by the deeper quantum well at

the edge.

The change in well thickness will affect the mobility directly. Interface roughness scattering can cause a strong reduction in mobility in quantum wells with decreasing widths [144]. The narrower well at the edge, as indicated by the TEM pictures, will experience increased interface roughness scattering and this will help lower the mobility.

Surface roughness scattering, which is dependent on the Ge fraction as well as the growth temperature and growth kinetics, has been shown to increase as the channel thickness decreases [138] ($\mu \propto d^{-6}$ where d is the channel thickness) [149]. This has a stronger effect near the wafer edge where the channel thickness is smaller. Theoretical calculations suggest that there is a strong increase in surface roughness as the Ge concentration increases [150] and the larger Ge fraction at the wafer edge will decrease the mobility through the increased surface roughness. In other research carried out, there is evidence that suggests that there will be a strong increase in surface roughness as the Ge concentration is increased [150]. AFM results show that there is a clear increase in the surface roughness near the wafer edge, where the Ge fraction is larger.

5.6 Conclusions

The radial thermal gradient across the substrate heater in the DERA UHV compatible CVD growth system, causes a variation in growth temperature of the substrate across the wafer. This has been shown to have a clear effect on the uniformity of any wafer structure grown in this system and hence the material properties.

Samples have been taken from across wafer 7B25, a Si/SiGe 2DEG wafer which possesses a regrowth interface, grown by DERA in the UHV compatible CVD system. TEM and SIMS images have been used to investigate the uniformity of the wafer structure. There is a noticeable change in the layer thicknesses as well as the Ge fraction in the SiGe layers across the wafer. Near the centre of the wafer, which has a higher substrate growth temperature, TEM images show the buffer regions and quantum well are thicker than the edge. SIMS data shows that the variation in temperature across the substrate leads to a difference in the Ge content and hence the quantum well depth but does not seems to effect the dopant concentration. The edge of the wafer has a higher Ge fraction and so has

a deeper quantum well than the wafer centre.

The change in structure permits an investigation into the effect of varying the layer thickness as well as the quantum well depth on the electronic properties, using samples obtained from the same wafer. All samples taken from 7B25 have been processed simultaneously and so any variation due to device processing or background growth conditions is expected to be minimal.

Electrical assessment of results show that there is a clear monotonic variation in the low temperature Hall mobility and carrier density across the wafer. There is a gradual decrease in the mobility and an increase in the carrier concentration going from the centre of the wafer to the edge.

TEM images and SIMS data show that not only is there a narrower and deeper Si quantum well at the edge of the wafer, but that there is also a smaller spacer thickness between the doped region and the quantum well. Since dopant concentration is fairly uniform across the wafer, this has the effect of increasing the carrier density towards the wafer edge.

The significant decrease in the Hall mobility as well as the mean free path of the electrons towards the wafer edge, indicate that there is increased electron scattering. The Si well at the wafer edge is closer to the dopant supply layer and so is more susceptible to remote ionised impurity scattering. The reduced spacer thickness between the quantum well and the regrowth interface will have a detrimental effect on the Hall mobility. The narrower well at the edge, indicated by the TEM pictures, will also reduce the mobility due to increased interface roughness scattering. AFM images show that there is more surface roughness at the wafer edge, related to the increased Ge fraction, which will also decrease the mobility. The increased effect of these different scattering mechanisms can explain the decrease in Hall mobility, towards the wafer edge.

This chapter shows the importance of growth temperature on the wafer structure and material properties. A small variation in wafer growth temperature has been shown to have a significant effect on the subsequent transport properties of samples. Within the limits of this analysis, it has been shown that optimum mobilities are obtained for samples which have wide quantum wells as well as large spacer thicknesses. Increasing the Ge content and hence the quantum well depth together with decreasing the layer thicknesses leads to greater carrier densities. Electron scattering mechanisms also have an increased effect and cause a decrease in the electron mean free path and hence reduce the low temperature

Hall mobility.

Since it was found that the highest mobility samples are ones closer to the wafer centre, all subsequent samples used for electrical assessment were taken from as close to the centre of the wafer as possible.

Chapter 6

Inverted 2DEGs Defined by *Ex-situ* Ion Implantation Doping

6.1 Introduction

6.1.1 Inverted Si/SiGe 2DEG Heterostructures

To form a 2DEG in the Si/SiGe system requires a n-type doped SiGe region in close proximity to a thin strained Si layer with a thin SiGe spacer between the two. Conventional 2DEGs are formed at the upper 'normal' interface or where the doped region is above the Si quantum well (see Figure 6.1). The 2DEG can also be formed at the lower 'inverted' interface of the SiGe/Si/SiGe quantum well, provided that there is a doped region below the Si quantum well (also shown in Figure 6.1). Traditionally, structures in the SiGe system grown by CVD have a conventional structure with the doped layer above the Si quantum well due to concerns over dopant segregation (further discussed in Section 6.1.2).

The fabrication of complex low dimensional devices requires effective gating action to control both the conductivity and the carrier density. In order to form a gated device in the Si/SiGe system a high quality SiO_2 layer is required. The growth of a high quality SiO_2 often requires high temperatures, which unfortunately can lead to diffusion and strain relaxation. Low temperature deposited oxides can be used but these have higher charge densities trapped at the interface which may screen any gate effect. To try and ensure that the oxide has a low den-

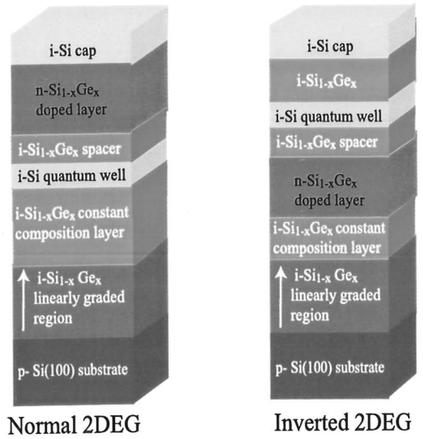

Figure 6.1: The structure of a conventional 2DEG structure, where the doped region is above the strained quantum well and an inverted 2DEG, where the doped region is below the strained Si well. The doped region is shown in red.

sity of interface traps, the wafer is normally capped with a thin Si layer. However this leads to problems when surface gates are used to vary the carrier density in the quantum well. If the Si cap is greater than 1 nm, the application of a positive bias may induce electrons into this region, resulting in parallel conduction.

In the n-channel Si/SiGe system, Schottky metal gating action has been limited by a large leakage current, partly caused by dopant segregation at the surface of the sample [141, 151]. One way to circumvent problems caused by surface gate leakage is to use an inverted structure, where the SiGe dopant supply layer is formed prior to the growth of the strained Si quantum well and any remaining heterolayers. Inverted heterostructures should help in minimizing any parasitic parallel conduction problems [152].

The ability to produce working inverted structure successfully has strong implications. There are many structures that have been investigated in the GaAs/AlGaAs material system that require two closely space quantum wells and require a doped region above the upper quantum well and below the lower quantum well. Such structures allow the investigation of electron-electron interactions and Coulomb drag [153]. In order to replicate these structures with Si/SiGe requires working inverted 2DEGs. If high quality inverted 2DEGs can be grown then this will allow the production of double channel heterostructures.

The major difficulty in growing n-type inverted modulation-doped structures

is the undesirable surface segregation of the n-type dopant and dopant memory problems in the growth chamber. If the dopant supply layer is below the Si well, segregation and diffusion of the n-type dopant can result in higher dopant densities in any subsequently grown layers (illustrated in Figure 6.2). Residual ionised impurities in the Si channel will act as scattering centres which can reduce the mobility and can lead to parallel conduction, thus negating the enhancements of modulation-doping [152, 125].

This chapter shows that it is possible to produce working devices from UHV-CVD grown Si/SiGe wafers, which have an inverted 2DEG structure. A novel technique is used that employs *ex-situ* ion implantation to form a dopant supply region together with the regrowth technique explored in chapter four.

6.1.2 *Ex-situ* Ion Implantation Doping and Regrowth

The doped regions in the samples presented in chapters four and five have been formed by introducing a dopant gas into the growth chamber during wafer growth. A doped region is formed in the heterostructure as result of growth kinetics. A consequence of gas source growth techniques is that residual traces of the dopant may remain in the chamber long after the initial introduction. These can lead to the contamination of all subsequent growth through surface segregation, memory effects and diffusion. One way of reducing contamination problems would be to ensure that the growth chamber and wafer surface are clean and that the growth chamber is constantly pumped. This is very difficult to achieve. Ideally, the best method would be to avoid the introduction of any dopant or other potential contaminant into the growth chamber. One solution to these problems is to introduce *ex-situ* doping of the wafer.

Chapter four showed results obtained for n-channel Si/SiGe heterostructures that had been formed by sequential growths of the virtual substrate and the channel layers separated by a chemical cleaning stage. It was shown that the introduction of a regrowth interface may not significantly affect the performance of fabricated devices and thus a SiGe virtual substrate may be treated in similar manner to any normal Si substrate. The feasibility of producing working devices from wafers that have been taken out and returned to a UHV compatible CVD chamber has been demonstrated in chapter four. This permits *ex-situ* processing of the virtual substrate, before active heterolayers are 'regrown'.

The use of high energy, *ex-situ* ion implantation in forming a dopant sup-

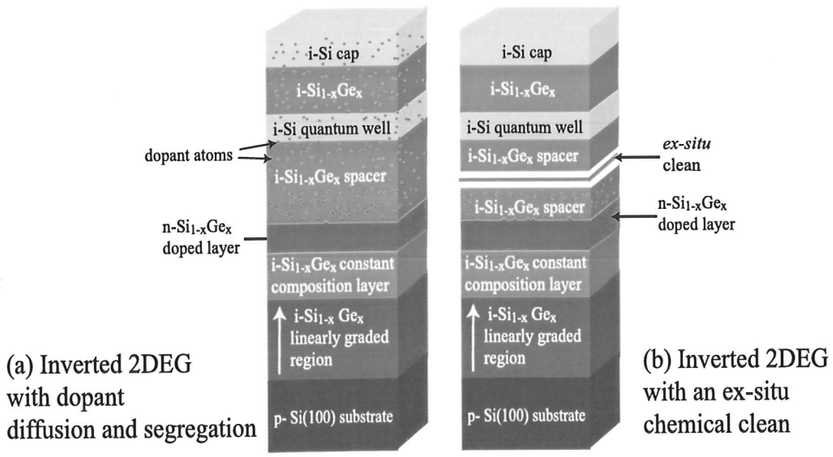

Figure 6.2: A schematic of an inverted 2DEG suffering from dopant diffusion and segregation compared to the structure of an inverted 2DEG that incorporates a regrowth interface.

ply layer is explored in this chapter. There are several issues that need to be addressed if this method is to be successfully used in large scale wafer productions. The relationship between the dopant ion penetration depth in the wafer and the incident ion beam energies needs to be established. In particular the ion dosage needs to be carefully tabulated to determine the dopant dose and carrier concentrations in subsequent devices.

Ex-situ ion implantation is not a viable method for providing dopants in conventional 2DEG structures. High energy ion bombardment may cause extensive damage to the wafer surface. Moreover the deep penetration range of some ions may disrupt and damage the underlying crystal structure. High temperature anneals are needed to recrystallize the structure after ion implantation. It is easier to recrystallize bulk Si or SiGe than a structure that includes a strained-Si quantum well or any strained layer. *Ex-situ* ion implantation doping is most suited to partially grown inverted structures whereby the active heterolayers are grown after the ion implantation and the high temperature anneal used to activate the dopant. Dopant penetration is not a major concern, since there will only be a bulk virtual substrate underneath the doped region. It is easier to recrystallize the bulk substrate and so residual implantation damage and any diffusion caused by the anneal will not affect the active heterolayers that are subsequently grown.

In the light of these challenges a new technique involving the *ex-situ* ion im-

plantation of dopants together with the regrowth technique outlined in Section 4.4 is explored in this chapter. Once a virtual substrate has been grown a thick protective oxide layer is deposited. The wafer is then removed from the growth chamber and *ex-situ* ion implantation is used to provide the n-type dopant. Next, the wafer is then chemically cleaned using the chemical cleaning procedure described in Section 4.4. The wafer is then returned to the CVD system for the growth of the remaining heterolayers, including the strained Si channel layer. An inverted structure incorporating a regrowth interface is shown in Figure 6.2.

This combined *ex-situ* ion implantation and regrowth technique circumvents the problem of dopant segregation in the CVD growth of MODFETs and has been used to obtain high mobilities in inverted n-type $Si/Si_{0.77}Ge_{0.23}$ heterostructures. Details of this technique will be presented together with results obtained from wafers produced using this procedure. These results have also been presented in two papers (see [154] and [155]).

6.2 DERA 7C Series Inverted Si/SiGe 2DEGs

Two different series of wafers were produced and each series consisted of three wafers. Each set of wafers were grown at the same time and samples from each wafer set were processed and tested concurrently to eliminate any fabrication and measurement related errors.

All of the wafers used in this study were grown using SiH_4 and GeH_4 mixed with H_2, on 100 mm 10 - 20 Ωcm p-type Si(100) substrates in the DERA UHV compatible CVD growth chamber described in chapter three. The wafers had the same basic structure, optimised for low-temperature electrical properties, as shown in Figures 6.3 and 6.6.

The first series, hereafter referred to as the 7C series, had two wafers (7C24 and 7C25) with p-$Si_{0.77}Ge_{0.23}$ virtual substrates grown on p-Si(100) substrates and one wafer (7C4) with a i-$Si_{0.77}Ge_{0.23}$ virtual substrate grown on a p-Si(100) substrate. The three wafers in the second series, hereafter referred to as the 8A series, were i-$Si_{0.77}Ge_{0.23}$ virtual substrates grown on a p-Si(100) substrates.

Each wafer was grown in two separate epitaxial stages. Initially a SiGe virtual substrate was grown. The wafers were removed from the growth chamber and an ex-situ protective oxide layer was deposited and dopant supply layers were formed by *ex-situ* ion implantation. There is a possibility that bombardment of the oxide with high energy ions may lead to some oxygen atoms being knocked on into the $Si_{0.77}Ge_{0.23}$ virtual substrate, but it was believed that any degradation

in electrical properties caused by this should be minimal and the oxide was used in order to minimise any damage to the wafer surface. After oxide removal and a subsequent chemical clean, the wafers were returned to the CVD chamber for the regrowth of the remaining heterolayers including the $Si_{0.77}Ge_{0.23}$ buffer, Si channel and the $Si_{0.77}Ge_{0.23}$ capping layers.

6.2.1 DERA 7C Series Structure

The DERA 7C wafers had $Si_{1-x}Ge_x$ virtual substrate linearly graded in Ge concentration from $x = 0$ to 0.23, over ~ 3.5 μm. In most virtual substrates that have been used to grow Si/SiGe 2DEGs in the course of this thesis, an undoped SiGe virtual substrate is grown on top of a p-Si(100) substrate. Instead of the usual undoped virtual substrate, 7C24 and 7C25 have a lightly doped p-type virtual substrate. It was hoped that any excessive n-type dopant diffusion and segregation would be compensated for by the presence of the p-type carriers. The p-type virtual substrates were also expected to minimize any problems caused by contamination by any n-type dopants that might have been present in the growth chamber.

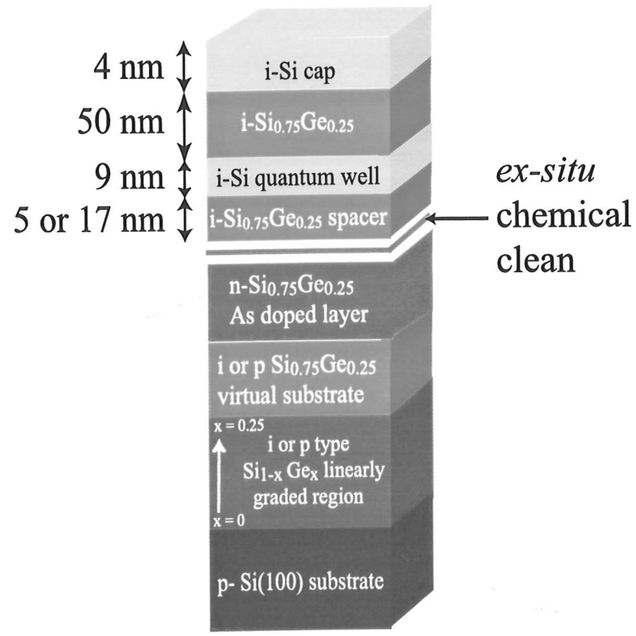

Figure 6.3: Basic structure of the 7C series n-channel inverted Si/SiGe 2DEG doped with $ex-situ$ ion implantation with a regrowth interface.

Once the desired Ge concentration of 23% was reached, a thick $Si_{0.77}Ge_{0.23}$ constant composition buffer of about 1 μm thickness was grown. Once the virtual substrates were removed from the growth chamber a thick SiO_2 layer about 40 nm thick was deposited on the surface of the wafer using plasma enhanced chemical vapour deposition (PECVD), after which they were ion-implanted with an n-type implant of arsenic. To try and determine the optimum structures for conduction at low temperatures and the ideal implant doses, modelling programmes and simulations were used to try and calculate the optimum structures.

Ion implantation of the wafers was carried out using a Varian 350RD. The angle of the incident beam was at 7° to the wafer surface to minimize any channeling effects (see appendix A) and all ion implantation was carried out at a temperature of 300 K. In order to maximise resources, each wafer in the first series was implanted at different energies on different parts of the wafer. Initially the entire wafer was implanted with 50 keV As at 1×10^{13} cm^{-2} by rastering the incident ion beam across the wafer. Then only half of each wafer was exposed to the same dose, N_D, of 1×10^{13} cm^{-2} As but with a higher implantation energy of 100 keV. The different implantation energies were used in order to see what effect implantation energy has on the electrical properties of the wafer.

These ion implantation energies and doses were carefully selected after the structure was modelled using TMA-Medici and Silvaco Supreme3 software[1]. Limitations of the growth system and ion implantation system were taken into consideration wherever possible. Simulation results for the inverted 2DEG structures are shown in Figure 6.4. The 7C series structure as shown in Figure 6.3 was used in this model. Structures with two spacer thickness of 5 nm and 17 nm with As implant energy of 100 keV and a range of doses between 1×10^{13} to 20×10^{13} cm^{-2} have been used. The expected carrier density is shown as a function of the As ion dose. It should be noted that the simulation does not account for the effects of a regrowth interface.

After implantation, the dopant was activated by a rapid thermal anneal (RTA). A high temperature is required to excite the dopant from interstitial sites into the lattice sites. Wafers 7C4 and 7C24 were annealed at a temperature of 850°C for a duration of 30 s. Wafer 7C25 was annealed at a slightly higher

[1]This was carried out by Dr A. C. Churchill at DERA

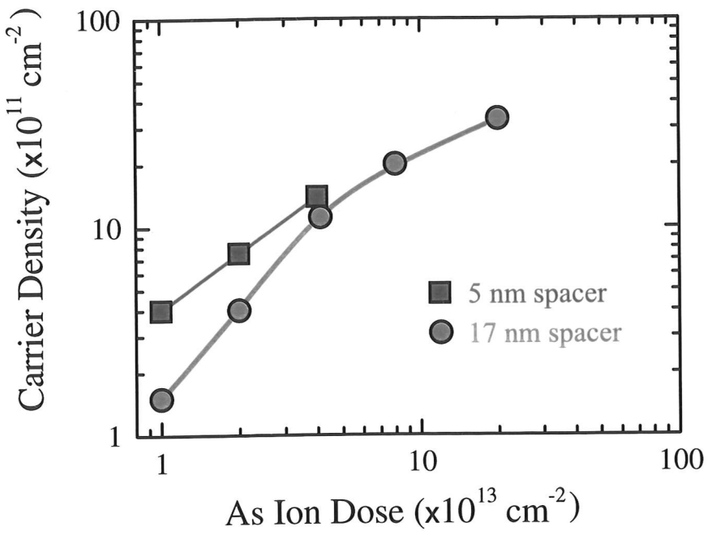

Figure 6.4: Simulation results showing the expected carrier density as a function of the As ion dose for the 7C inverted 2DEG structure. This figure was obtained with TMA-Medici software and ion implant models of Silvaco Supreme3 software.

temperature of 900°C for a duration of 30 s. After the anneal the cap oxide was then removed from the substrates using 1:10 HF:H_2O, then chemically cleaned in a FSI Mercury spray cleaner using the proprietary B2/CLEAN/R2 recipe described in detail in chapter four.

The wafers were returned to the UHV compatible CVD system where any residual oxide was desorbed in H_2 at a temperature of 800°C and at a pressure of 130 Pa for 8 minutes. The pressure and temperature were then reduced and an undoped $Si_{0.77}Ge_{0.23}$ spacer, d_{sp}, with varying thickness was grown. The wafer with the undoped virtual substrate, 7C4, was given a thin 5 nm spacer whilst the other 2 wafers with the p-type virtual substrates (7C24 and 7C25) both had a larger 17 nm spacer. The larger spacer thickness of 17 nm has been used successfully in conventional modulation-doped 2DEGs to reduce the effects of remote ionised impurity scattering [58] at low temperatures. All of the wafers had an i-Si channel, 9 nm thick, considerably less than the Matthews and Blakeslee critical thickness for strained-Si on $Si_{0.77}Ge_{0.23}$ [23]. Finally, a 50 nm undoped $Si_{0.77}Ge_{0.23}$ layer was grown with a nominally 4 nm Si cap.

Details of the 7C series structure are given in Table 6.1. Samples from the

Wafer	Substrate type	Implant energy (keV)	Spacer thickness (nm)	RTA temperature (°C)
7C4a	i-$Si_{0.77}Ge_{0.23}$	50	5	850
7C4b	i-$Si_{0.77}Ge_{0.23}$	100	5	850
7C24a	p-$Si_{0.77}Ge_{0.23}$	50	17	850
7C24b	p-$Si_{0.77}Ge_{0.23}$	100	17	850
7C25a	p-$Si_{0.77}Ge_{0.23}$	50	17	900
7C25b	p-$Si_{0.77}Ge_{0.23}$	100	17	900

Table 6.1: Summary of the different parameters for the DERA 7C series. All of these wafers were *ex-situ* ion-implanted with As at 1×10^{13} cm^{-2}

centres of each wafer section were fabricated into Hall bars, (described in Section 3.3). Annealed Au (1% Sb)/NiCr/Au (1% Sb) metal was used for the n-type ohmic contacts for the first series of wafers. Full details of the growth are also given in [154, 155].

6.2.2 DERA 7C Series Results

Extensive magnetotransport measurements were carried out on samples from all six wafer sections both in the dark and after extended illumination using a red LED. Measurements were carried out at room temperature, 77 K and 1.5 K.

All of the samples from wafers 7C24 and 7C25 did not conduct at room temperatures or at lower temperatures down to 1.5 K, irrespective of the ion implantation energy. The lower energy sample from the wafer with the undoped virtual substrates and the smaller 5 nm spacer, 7C4a (implanted at 50 keV as shown in Table 6.1) failed to conduct. However the 100 keV implant energy sample from wafer 7C4 (sample 7C4b) did conduct after extensive illumination.

A sample from 7C4b showed clear SdH oscillations and quantum Hall effect plateaux at 1.7 K, but did not give reproducible mobilities for measurements without illumination. Figure 6.5 shows magnetotransport results at 1.7 K for sample 7C4b. A Hall mobility of 73 000 $cm^2V^{-1}s^{-1}$ for a carrier concentration of 4.25×10^{11} cm^{-2} was obtained. The simulation results presented in Figure 6.4 gave an estimate for the carrier density as $\sim 4 \times 10^{11}$ cm^{-2}. The value of the real carrier density is slightly higher than the simulation but was obtained after the sample was illuminated.

All of the samples that had the lower 50 keV energy failed to conduct at

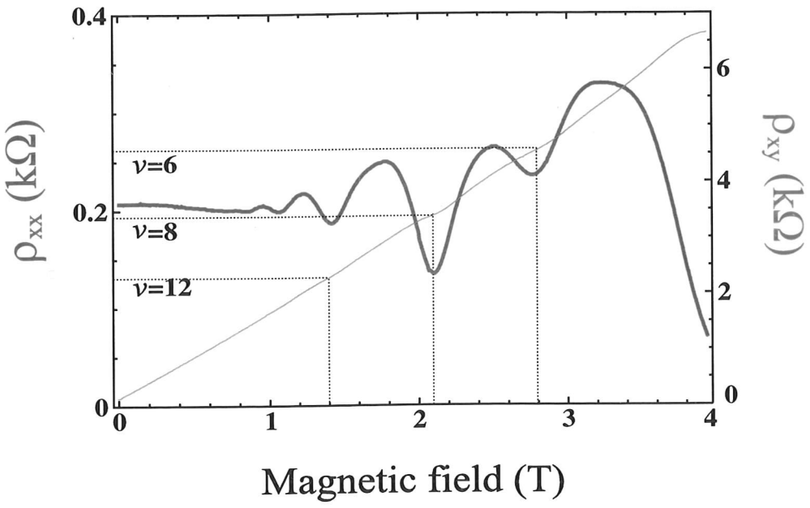

Figure 6.5: Longitudinal (ρ_{xx}) and Hall (ρ_{xy}) resistivity results for DERA Wafer 7C4b. This sample has been *ex-situ* ion implanted with As at 1×10^{13} cm^{-2} at 100 keV. These results have been obtained after extended illumination with a red LED at 1.5 K.

all. Since the only working sample had a higher implantation energy, the most likely reason is that a 50 keV implantation energy is too low and that higher energies may be required. The conduction in sample 7C4b shows that an 850°C anneal should be high enough to activate the dopant and that higher temperature anneals are not necessarily beneficial. Wafer 7C25 was annealed at 900°C and samples from this wafer did not conduct even after prolonged illumination.

The spacer thickness, d_{sp} is shown to have an important effect on the electronic properties. If the spacer thickness is too large then an insufficient amount of carriers transferred from the modulation-doped layer for conduction. This is shown by the lack of conduction in the samples with the larger 17 nm spacers. Only sample 7C4b, from the wafer that had been implanted at 100 keV and with a small 5 nm spacer provided results and then only after photo-exciting the electrons by extensive illumination. The lack of conduction without electron photo-excitation could be due to the presence of electron traps created either by ion implantation damage or at the growth interrupt where *ex-situ* cleaning has occurred. It most probably due to an insufficient amount of carriers transferred from the modulation-doped layer and that a 1×10^{13} cm^{-2} As dose is barely sufficient.

6.3 DERA 8A Series Inverted Si/SiGe 2DEGs

6.3.1 DERA 8A Series Structure

In order to optimise the structure for conduction at low temperature, in-house self-consistent Schrödinger-Poisson programs were used to determine the ideal energy and dose of implanted ions. The computer modelling programs and the simulation results shown in Figure 6.4, indicate that there may be increased carrier density with an increase in implantation dose. The results from the 7C series showed that a dose of 1×10^{14} cm^{-2} provides an insufficient amount of dopant for conduction. Therefore, the second series of wafers were all ion-implanted with an increased dopant dose.

The 8A series of wafers have a similar structure to the 7C series and Figure 6.6 shows the basic structure. The wafers from the 8A series were grown on a p-Si(100) substrate and undoped $Si_{0.77}Ge_{0.23}$ virtual substrates. 8A series wafers were also *ex-situ* ion implanted with As at 100 keV with a higher range of doses, N_D, of 2, 4 and 8×10^{13} cm^{-2}. Following ion implantation the substrates were annealed in a RTA at 850°C for 30 s. The protective oxide cap was stripped before the wafers were chemically cleaned and returned to the growth chamber.

Upon their return to the UHV compatible CVD system, all residual native oxide was removed by an 800°C oxide desorption for 10 minutes in 130 Pa of

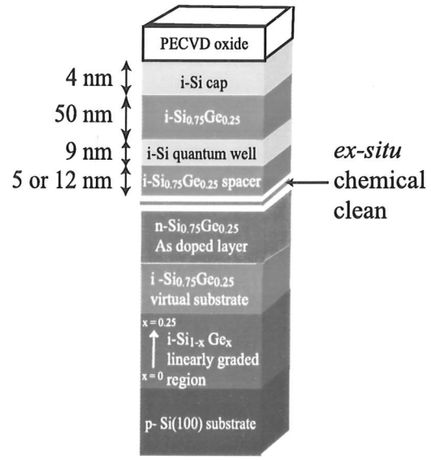

Figure 6.6: Basic structure of the 8A series n-type inverted Si/SiGe 2DEG with a regrowth interface.

Wafer Name	Substrate type	Implant Dose $\times 10^{13}$ cm^{-2}	Spacer thickness (nm)
8A1	i-$Si_{0.77}Ge_{0.23}$	2	5
8A2	i-$Si_{0.77}Ge_{0.23}$	4	12
8A3	i-$Si_{0.77}Ge_{0.23}$	8	12

Table 6.2: Summary of the different types of wafers in the DERA 8A series. All of these wafers were *ex-situ* ion-implanted with As at 100 keV

H_2. The remaining heterolayers were grown at a reduced pressure of 20 Pa and temperature of 600°C.

Two different i-$Si_{0.77}Ge_{0.23}$ spacer thicknesses were used. The 7C series shows that the spacer thickness, d_{sp} has an important effect on the electronic properties. Since the only working sample from the 7C series had a thin 5 nm spacer, the substrate with the lowest dose of 2 $\times$ 10^{13} cm^{-2} of As was also given a thin 5 nm spacer. The other two higher dose substrates were expected to have a greater dopant density in the doped region of the wafer and so were given thicker 12 nm spacers in order to reduce the effects of remote ionised impurity scattering in the 2DEG layer above. A summary of the different dopant concentrations and energies and the spacer thickness are presented in table 6.2.

All of the wafers had a 9 nm i-Si channel and finally a 50 nm undoped $Si_{0.77}Ge_{0.23}$ layer was grown with a nominally 4 nm Si cap. The 8A series wafers had a Plasma Enhanced CVD oxide (annealed at a temperature of 850°C) grown on them for protection. Later the oxide was removed and Al(1% Si) metal was deposited on the wafer surface in order to form ohmic contacts.

Wafer Name	N_D $\times 10^{13}$ cm^{-2}	d_{sp} nm	μ cm^{2}V^{-1}s^{-1}	n_s $\times 10^{11}$ cm^{-2}	τ_q ps	α	l μm
7C4a	1	5	73 000 *	4.25*	1.9*	4.3*	0.79*
8A1	2	5	35 000	10.5	0.7	5.3	0.59
8A2	4	12	28 000	7.38	1.1	2.9	0.40
8A3	8	12	15 000	14.5	-	-	0.29

Table 6.3: Growth parameters and transport characteristics at 1.7 K for the inverted Si/$Si_{0.77}Ge_{0.23}$ heterostructures. Values marked with * were obtained after illumination. τ_q, α and l are defined in sections 6.3.2 and 6.3.2.

6.3.2 DERA 8A Series Results

Magnetotransport Results

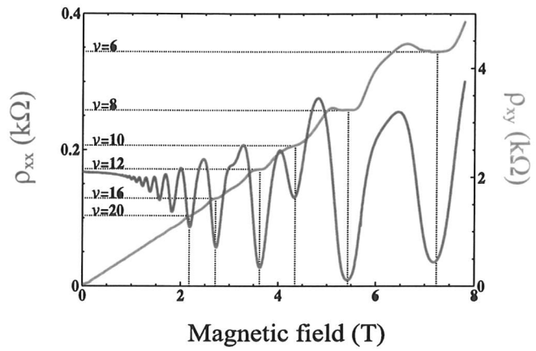

Figure 6.7: Longitudinal and Hall resistivities at 1.7 K for inverted samples 8A1 (with n = 10.51 $\times$ 10^{11} cm^{-2} and μ = 35 000 cm^{2}V^{-1}s^{-1}).

Low temperature transport properties could be extracted without illumination for all samples from the 8A series of wafers and these are summarised in Table 6.3. Sample 7C4b with As dose N_D= 1 $\times$ 10^{13} cm^{-2} implanted at 100 keV, has been illuminated with a red LED and is included here for comparative purposes.

At 1.7 K, carrier densities ranging from 4.25 $\times$ 10^{11} cm^{-2} to 1.45 $\times$ 10^{12} cm^{-2} and mobilities ranging from 15 000 cm^{2}V^{-1}s^{-1} to 73 000 cm^{2}V^{-1}s^{-1} were obtained. The longitudinal (ρ_{xx}) and Hall resistivity (ρ_{xy}) in an applied perpendic-

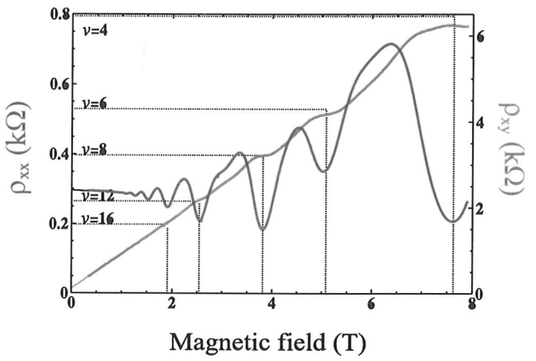

Figure 6.8: Longitudinal and Hall resistivities at 1.7 K for inverted samples 8A2 (with n = 7.38 $\times$ 10^{11} cm^{-2} and μ = 28 000 cm^{2}V^{-1}s^{-1}).

ular magnetic fields up to 8 T for samples 8A1 and 8A2 are shown in Figures 6.7 and 6.8. The samples show well-defined SdH oscillations in ρ_{xx}. Cyclotron-split Landau levels are resolved at a filling factor of $\nu = 36$ and spin-split Landau levels at $\nu = 14$. Quantum Hall effect plateaux are observed in ρ_{xy} above 1.8 T at 1.7 K.

Mean Free Path

In the CVD growth system used to produce these wafers, the mobility of 2DEGs has been shown to depend strongly on the carrier density in the system. Therefore for a more accurate picture the electron mean free path (l), may be more informative. Figure 6.9 depicts the calculated mean-free path as a function of the ion dose. The plot clearly shows a trend of lower mean-free path as the dose is increased, irrespective of spacer layer thickness.

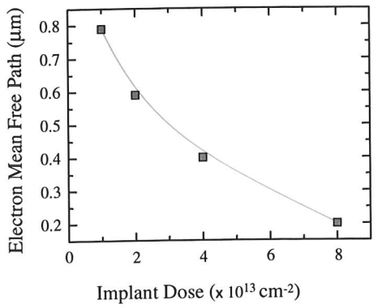

Figure 6.9: Mean free path versus ion implantation dose plotted using data obtained from Si/SiGe inverted 2DEGs. The solid line is a guide to the eye.

Quantum Lifetime Measurements

The quantum lifetime, τ_q, reflects the broadening of the Landau levels and can be derived from the magnetic field dependence of the amplitude of the SdH oscillations as discussed in Section 2.5.4. As stated in chapter two, Dingle plots are constructed of $\ln[(\Delta\rho_{xx}/\rho_o)(\sinh(\chi)/\chi)]$ versus 1/B where $\Delta\rho_{xx}$ is the amplitude of the oscillation, ρ_o is the zero field resistivity and $\chi = 4\pi^2 k_B T/(eB)$ [82]. Figure 6.10 is a Dingle plot plotted using data taken at 1.7 K for samples from wafers 7C4b, 8A1 and 8A2. The values of τ_q that are obtained range from 0.7 ps to 1.9 ps (refer to Table 6.3).

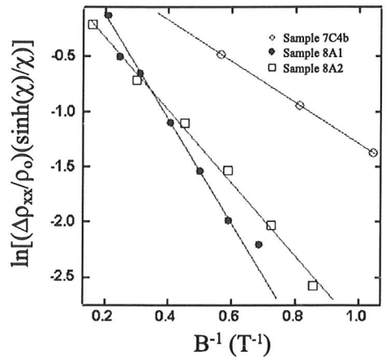

Figure 6.10: Dingle plots at 1.7K for samples 7C4b, 8A1 and 8A2. The slope of the graph is given by -πm*/($e\tau_q$). The values of τ_q obtained are shown in Table 6.3 and this figure has been presented in [155]

The ratio of the transport relaxation time to the quantum lifetime was found to be $\alpha = 2.9$ to $\alpha = 5.3$ for samples 7C4b, 8A1 and 8A2. In chapter five, α values ranging from 2.9 to 8.44 were found for higher mobility non-inverted n-type $Si/Si_{0.77}Ge_{0.23}$ heterostructures. As before, these values indicate the predominance of several possible scattering mechanisms such as remote ionised impurity scattering and surface roughness scattering. However, other factors such as regrowth interface scattering should not be ignored.

6.4 Discussion of Results

The spacer thickness between the doped region/regrowth interface and the strained Si well is very important. The sample results in chapters four and five have shown that as the regrowth interface approaches the well, the carrier density is reduced. However, the results in Section 6.2.2 show that in inverted Si/SiGe 2DEGs, if the spacer thickness is too large then there will be an insufficient density of carriers in the quantum well for conduction. Even if a very thin spacer is used, it may still not be possible to produce a working device, if the implant dose and energy are low.

As the spacer thickness decreases between the doped region and the quantum well, it should be easier to excite carrier into the well, which would be expected to increase the carrier density. However the increased proximity of the doped region to the quantum well will lead to an increase in remote ionised impurity

scattering. As the regrowth interface is brought closer to the well it will increase the surface roughness in the quantum well. In chapters four and five it is also suggested that the interface itself may contain charged traps, which have a detrimental effect on the mobility and carrier density. This can only be improved by further research into improved wafer surface morphology after the ion implantation and chemical cleaning stage. Due to a shortage of resources, this has not been possible during this thesis.

As a general trend, an increase in the dopant dose leads to an increase in the carrier concentration and a reduction in the mobility. Measurements made in the dark show a clear linear relationship between the mobility and the As concentration. If the dopant is below about 2×10^{13} cm^{-2}, it is difficult to excite carriers into the quantum well and low temperature conduction may only possible after the electrons have been photo-excited. This could be due to an insufficient amount of carriers transferred from the modulation-doped layer. It may also be due to the presence of electron traps created either by ion implantation damage or at the growth interrupt where *ex-situ* cleaning has occurred and chapter four shows that a regrowth interface may contain electron traps that limit the carrier density. However, as the dopant concentration increases, other scattering mechanisms begin to effect the mobility and carrier concentration in the quantum well.

Table 6.3 shows that for a given spacer thickness, as the ion dose increases, so does the sheet carrier density in the strained Si well. However, as the carrier

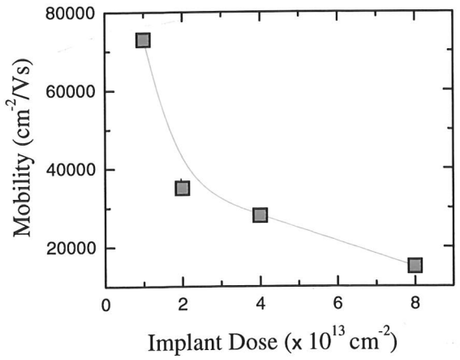

Figure 6.11: Hall mobility versus ion implantation dose plotted using data obtained from Si/SiGe inverted 2DEGs. The solid line is a guide to the eye.

density increases, the mobility falls. The results imply that the mobility of the samples could either be affected by remote ionised impurity scattering or interface roughness scattering.

The mean-free path is observed to decrease with increasing ion dose, irrespective of spacer layer thickness as shown in Figure 6.11. It would be expected that the larger carrier density should increase electron screening, which ought to result in a greater mean free path. The more plausible cause for the decrease in mean-free path as ion dose increases is interface roughness scattering on the lower interface of the strained Si layer and the underlying SiGe alloy layers. As the sheet carrier density in the strained Si quantum well increases, the electron Fermi wavelength decreases and so the sensitivity to interface roughness increases.

6.5 Conclusions

In this chapter a combined *ex-situ* ion implantation and regrowth technique has been used to produce inverted Si/SiGe 2DEG structures. This study has shown the feasibility of using *ex-situ* ion implantation as a means of providing a modulation-doped layer in inverted n-type Si/$Si_{0.77}Ge_{0.23}$ heterostructures. The *ex-situ* doping circumvents the need to introduce dopants into the growth chamber and hence circumvents dopant segregation during growth. This enables samples with Hall mobilities of up to 73 000 cm^{2}V^{-1}s^{-1} for a carrier concentration of 4.25×10^{11} cm^{-2} to be achieved. Samples tested in magnetic fields of up to 8 T at 1.7 K showed clear SdH oscillations and quantum Hall effect plateaux, demonstrating the quality of this fabrication technique.

It has been shown that the ion implantation of dopants into SiGe virtual substrates does not prevent the deposition of subsequent heterostructure layers. Within the limits of the analysis in this chapter, a relationship between the implanted ion concentration and the transport properties is evident. If the ion implantation energies and dose are low, then it may not be possible to produce working devices. If the ion dose is less than 2×10^{13} cm^{-2}, low temperature conduction may only occur after the electrons have been photo-excited. Increasing the dose causes a corresponding increase in carrier density in the quantum well. However, as the carrier density increases, there is a decrease in mobility.

the mobility to fall.

This chapter also emphasises the significance of the spacer thickness between the quantum well and the dopant supply layer in inverted structures. In the inverted Si/SiGe 2DEG structures used in this chapter, the incorporation of a regrowth step complicates the situation by adding a regrowth interface at the edge of the doped region. It has been shown that if the spacer thickness used are too large, then an insufficient amount of carriers will be transferred from the doped region to the quantum well for conduction.

Reducing the spacer thickness has the combined effect of bringing the dopant supply layer closer to the quantum well and bringing the regrowth interface closer to the quantum well. Bringing the quantum well closer to the dopant supply layer makes it easier for carriers to populate the quantum well but also increases remote ionised impurity scattering. The regrowth interface has a detrimental effect on the material properties and bringing the regrowth interface closer to the quantum well, will reduce both the carrier density and the Hall mobility. A more detailed analysis of the relationship between the spacer thickness and the transport properties has not been possible in this thesis. However it can be seen that the highest mobility samples have been obtained from wafers which have a small 5 nm spacer thickness.

The *ex-situ* ion implantation and regrowth technique supports the idea that virtual substrates can be treated like conventional Si substrates. It has been shown that it is possible to incorporate *ex-situ* processing steps, such as ion implantation of dopants and still yield working devices. The possibility of incorporating more elaborate *ex-situ* processing steps are further explored in the next chapter.

Chapter 7

Selective Area Doping using *Ex-situ* Ion Implantation and Regrowth

7.1 Introduction

Chapter four showed that by using a regrowth process it is possible to treat a virtual substrate like a standard Si substrate. Chapter six showed that it is possible to combine regrowth with *ex-situ* ion implantation to provide dopants in a Si/SiGe wafer and the necessity for using inverted structures was also discussed. In this chapter the *ex-situ* ion implantation and regrowth process is combined with electron beam patterning to form selectively defined doped regions within a Si/SiGe 2DEG wafer.

The feasibility of using ion-implanted P to form a conducting path to the 2DEG region is also explored in this chapter. Ion implanted ohmic contacts can be used together with selective area *ex-situ* ion implantation of the dopant to simplify device processing.

The modified *ex-situ* ion implantation process begins with the growth of a virtual substrate on which a thick oxide is deposited *ex-situ* by PECVD. The technique outlined in this chapter involves more extensive *ex-situ* processing. A resist is applied, which is pattern by an electron beam and then developed. During subsequent As ion implantation, only resist areas that have been developed will allow ions to penetrate through to the underlying SiGe virtual substrate. After ion-implantation, the wafer is annealed and then chemically cleaned (as discussed

in Section 4.4), before it is returned to the UHV compatible CVD chamber for the growth of the remaining heterolayers. Finally doses of 8×10^{14} cm^{-2} of P were implanted at 180 keV and activated an 850°C anneal for 30 s, to form low resistance ohmic contacts. The implantation energy and dose as well as the anneal temperature and duration for the P ohmic contacts is discussed in detail in Section 7.3.

Electron beams have high resolutions and allow the patterning of very small areas and have been used to define Hall bar shapes normally used in the assessment of material quality. The selective area, ion implanted 2DEG region circumvents the need to physically etch a mesa during device processing and subsequent device processing is simplified significantly. The successful application of this *ex-situ* selective area doping technique is demonstrated in this chapter.

The ability to define very small doped areas has been used to fabricate devices with constricted regions as small as 200 nm, in the Hall bar pattern. The final section of this chapter discusses the use of this selective area patterning and doping technique in forming devices with small scale geometries. Results from conductance measurements from working devices that have constrictions of 500 nm are presented and limitations of the current technique are also discussed.

7.2 Modified Wafer Growth Process

The *ex-situ* selective area ion implantation technique utilises a modified wafer growth technique outlined below in Section 7.2.1. Subsequent device processing is slightly different to the one normally used for device fabrication (as described in Section 3.3) and a summary of the modified routine is outlined in Section 7.4.2.

7.2.1 Selective Area Ion Implantation and Wafer Regrowth

One drawback in using the UHV compatible CVD growth system and the ion implantation system at DERA that is used for research, is that these systems cannot easily accommodate small wafer segments. Therefore the technique that has been developed here is a whole wafer process. The selective implantation process requires the accurate positioning of alignment marks on the wafer surface.

Chapter six showed that when using ion implantation to create a doped region in a wafer, an inverted structure is preferred. The wafers that were used, were grown on 100 mm p-type (10-20 Ωcm) Si(100) substrates in the UHV compatible

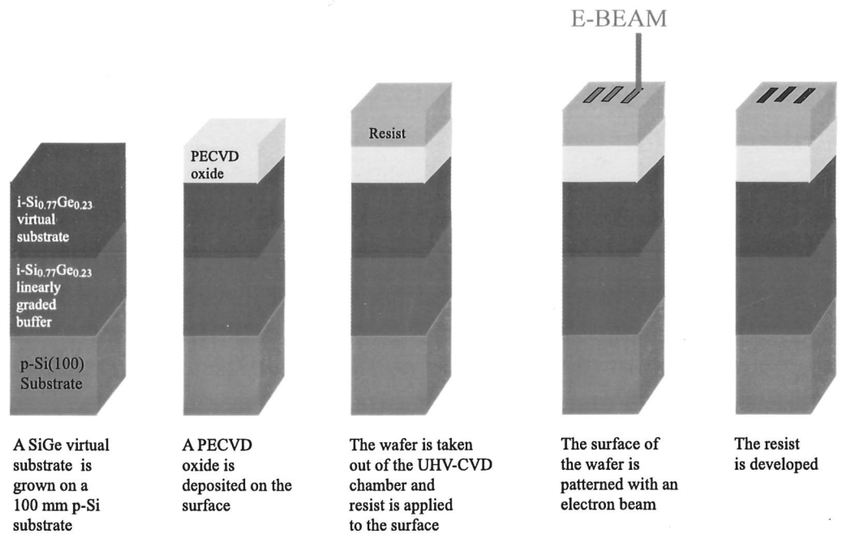

Figure 7.1: The initial stages in the growth of the selective area dopant patterning process are shown.

CVD growth chamber described in Section 3.2.1. Initially a 3.5 μm linearly graded $Si_{0.77}Ge_{0.23}$ alloy is grown followed by a ~ 1 μm constant composition $Si_{0.77}Ge_{0.23}$ layer. At this point the wafer is removed for *ex-situ* processing and a protective PECVD oxide is grown before.

Figure 7.1 shows the selective area patterning process. Initially a thick resist is applied to the wafer surface above the oxide. The implanted ions should be unable to penetrate through the undeveloped resist. The resist has to be thick enough to absorb all incident ions in undeveloped regions.

7.2.2 Selective Area Electron Beam Patterning and Ion Implantation

The wafer is now ready for patterning with an electron beam. The electron beam system used by DERA is a Leica Cambridge Instruments EMBF 10.5 CS120 system, which allow the definition of features down to 0.1 μm. It is used to pattern the deposited resist in selected areas to define Hall bar shapes. A 2 μm thick Shipley resist is applied and is developed for 60 s. Only regions that have been developed should allow ion penetration to occur in the subsequent implant stage and hence there should be a well defined shape. Any divergence in the electron

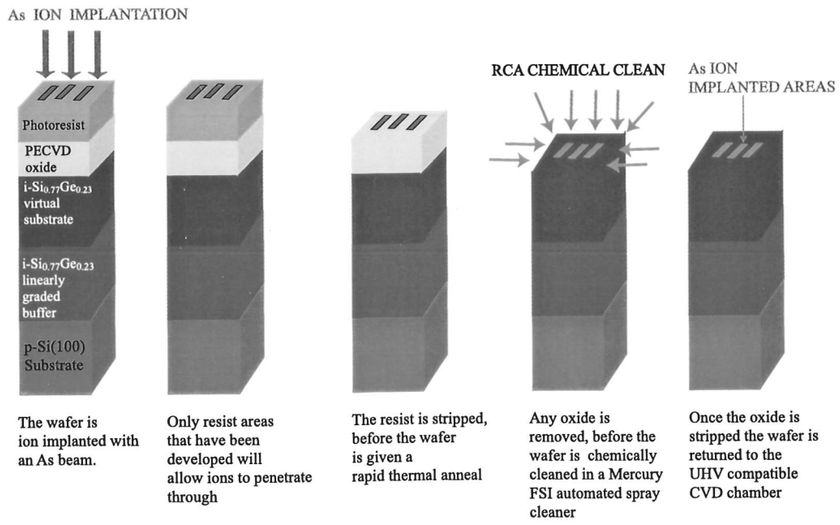

Figure 7.2: The remaining steps in the $ex - situ$ selective are dopant patterning process are shown.

beam or spreading of implanted ions should be minimal and the patterning process is expected to produce the desired features. Given the statistical nature of ion implantation and the variable penetration ranges of incident ions (see appendix A), some ions will be able to penetrate through the undeveloped resist and the deposited oxide down to the bulk $Si_{0.77}Ge_{0.23}$. However, the number of such ions will be minimal and should not be large enough to significantly dope the wafer. Only the intentionally ion implanted regions have a large enough dopant concentration to significantly alter the electronic properties of the material.

The entire wafer has to be patterned at once, resulting in the whole wafer surface being covered in Hall bar shapes, each carefully positioned. It would take a long time to pattern the whole wafer with a fine resolution electron beam. Therefore, a broad beam is initially used to define larger features before a fine beam with a smaller spot size is used to define smaller features. It is possible to see well defined Hall bar shapes on the wafer surface using a microscope at the end of the patterning process.

The remaining steps in the wafer growth process are shown in Figure 7.2. The first stage shown in Figure 7.2 is the ion implantation of the wafer. Once the resist has been developed, it is exposed to an As ion beam, which is evenly

rastered across the whole surface. Each wafer has a slightly different dose of either 2 or 4 $\times$ 10^{13} cm^{-2} of As and have been ion implanted at 100 keV.

After implantation, the resist is removed and the wafers are annealed. The oxide is left on the wafer surface during the anneal to protect the wafer from any remaining metal ions which might drive-in during the annealing process. The substrates are annealed at 850°C for 30 s, in order to activate the dopant and to recrystallize the bulk SiGe.

Once the oxide is stripped the substrate is chemically cleaned using the B/CLEAN/R2 process followed by a HF oxide strip, described in Section 4.4. The wafer can be inspected under a microscope to see whether any Hall bar features and alignment marks are visible. During the growth of the wafers used in this study, the surface clearly showed small well defined regions that had been patterned (typical small features that are defined using this technique are shown in figure 7.10). The virtual substrate showing ion implanted Hall bar shapes is returned to the growth chamber.

It is possible for the entire wafer surface to be flood implanted if all incident ions penetrate through to the underlying $Si_{0.77}Ge_{0.23}$ surface, which would negate the selective area patterning. One test to see if this has occurred is to take a sample of material from a part of the wafer that ought to be undoped and to check for conduction. This was carried out with samples from all wafers used in this study. All such samples showed no signs of conduction, further verifying the accuracy of the selective implantation process.

7.2.3 Regrowth of the Inverted 2DEGs

After the patterning and ion implantation stage, wafers are returned to the UHV compatible CVD growth chamber and any remaining oxide is desorbed at 800°C for 10 minutes in 130 Pa of H_2. Then the remaining heterolayers are grown at reduced pressure of 20 Pa and temperature of 600°C. The structure of the wafer is shown in Figure 7.3. Wafers with the lowest dose of As *i.e.* 2 $\times$ 10^{13} cm^{-2}, have 5 nm $Si_{0.77}Ge_{0.23}$ spacers. The other wafers with a larger dose of 4 $\times$ 10^{13} cm^{-2}, possess 12 nm $Si_{0.77}Ge_{0.23}$ spacers. Every wafer has a 9 nm Si quantum well followed by a 50 nm $Si_{0.77}Ge_{0.23}$ layer before the wafer is finally capped with 4 nm of Si. A PECVD oxide has been deposited on the wafer surface for protection during P ion implantation.

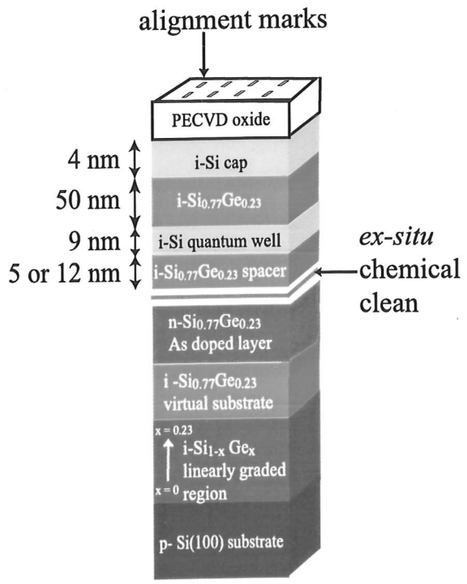

Figure 7.3: Basic structure of the selective area ion implanted inverted Si/SiGe 2DEGs with a regrowth interface.

7.2.4 Surface Alignment Marks and P Ion Implanted Ohmic Contacts

Once the oxide has been deposited, no visible signs of ion implantation remain on the wafer surface, which would make device fabrication almost impossible. Hence, a series of alignment marks are patterned along with the ohmic contacts with a P ion beam. The whole wafer needs to be positioned with extreme care to ensure that the P ion implanted regions overlap the electron beam defined As contact areas on the Hall bar. Any misalignment at this stage would make any subsequent device fabrication and assessment futile.

The implantation dose and energy used for the ohmic contacts is 8×10^{14} cm^{-2} at 180 keV, which is the peak dose and energy found in Section 7.3. Finally the wafers were annealed at 850°C for 30 s in order to activate the dopant.

7.3 P Ion Implanted Ohmic Contacts

In order to successfully use ion implanted P atoms to form a conducting path to a patterned 2DEG, time was spent developing ion implanted contacts that would be suitable for low temperature operation. Research was carried out on the effect of different ion implantation energies, doses and RTAs on the resistance of ion implanted ohmic contacts. Various in-house modelling and simulation programmes were utilised in order to try and calculate the optimum implantation dose and energy. Figure 7.4 shows a typical simulation result. Figure 7.4 shows the expected carrier density as a function of depth for different implantation energies of As and P ions, into unannealed Si. All of the simulations in Figure 7.4 have a dose of 8×10^{14} cm^{-2} and this figure was obtained with TMA-Medici software and ion implant models of Silvaco Supreme3 software. Also plotted is the experimental carrier density obtained using samples from 7B22.

Sample Number	Implantation Dose (10^{14} cm^{-2})	Implantation Energy (keV)	Anneal Temperature (°C)	Anneal Duration (s)
A1	4	100	750	30
A2	4	100	850	60
A3	4	100	850	30
A4	4	100	900	30
B1	4	180	750	30
B2	4	180	850	60
B3	4	180	850	30
B4	4	180	900	30
C1	8	100	750	30
C2	8	100	850	60
C3	8	100	850	30
C4	8	100	900	30
D1	8	180	750	30
D2	8	180	850	60
D3	8	180	850	30
D4	8	180	900	30

Table 7.1: A summary of the structure of the different samples used in the ion-implanted ohmic contact study. The different ion implantation doses and energies together with the anneal temperature and duration are listed.

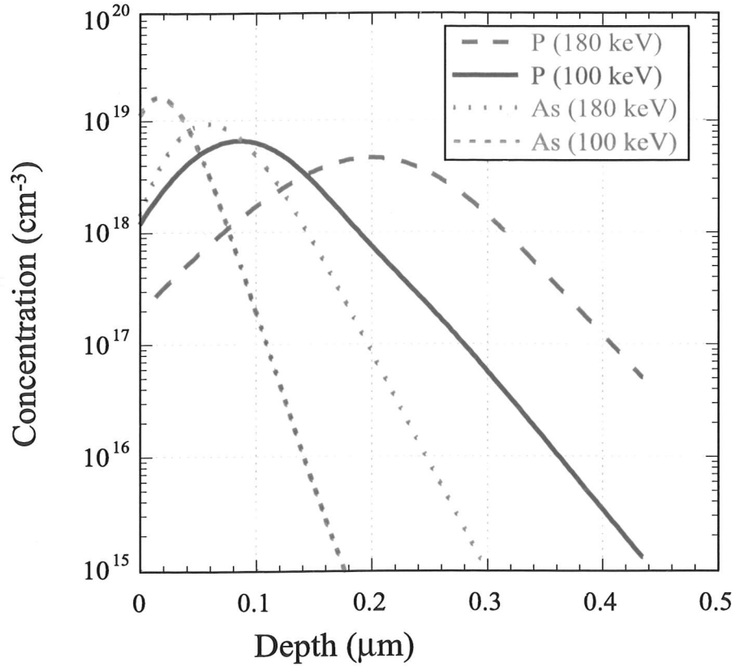

Figure 7.4: Simulation results showing the expected carrier density as depth for As and P ions (with a dose of 8×10^{14} cm^{-2}) into bulk Si. This figure was obtained with TMA-Medici software and ion implant models of Silvaco Supreme3 software.

Based on the results of these simulations, four identical different bulk i-$Si_{0.77}Ge_{0.23}$ wafers were implanted with P using differing doses and implantation energies.

The samples were prepared using the technique outlined in chapter three. Each wafer had a thick 40 nm protective SiO_2 layer deposited on the surface using PECVD to try and reduce damage to the wafer surface during wafer irradiation. Each of the four whole wafers was implanted with P with a slightly different ion implantation energy of either 100 or 180 keV and dose, N_D of either 4×10^{14} cm^{-2} or 8×10^{14} cm^{-2}.

After implantation the oxide was stripped and the wafer surface was chemically cleaned to remove any residual oxide. Each wafer was then cut into four quarters. Individual sections from were annealed with a slightly different anneal temperature and duration to activate the dopant. The anneal temperature used are close to the ones that are normally used in wafer growth varied from 750 °C

to 900°C for either 30 or 60 s. Details of the different ion implantation doses and energies together with the anneal temperature and duration are presented in table 7.1.

After the anneal the wafer surfaces were cleaned and Al with 1% Si surface ohmic contacts were deposited. Samples were then electrically assessed at room temperature and at 4 K. Sheet resistance (R_{sheet}) measurements were taken while passing a 100 nA current through the device. These results are summarised in table 7.2.

The lowest R_{sheet} values were obtained from samples that had been given a slightly higher dose of 8×10^{14} cm^{-2} both at 100 keV and at 180 keV (wafers C and D). Table 7.2 shows that all samples from wafer A, implanted with 4×10^{14} cm^{-2} P at 100 keV, did not conduct at room temperature or at lower temperatures. Wafer B has a similar dose but has been implanted at a higher

Sample Number	Measured RT Current (nA)	RT R_{sheet} Ω	4 K Current (nA)	4 K R_{sheet} (Ω)
A1	-	-	-	-
A2	-	-	-	-
A3	-	-	-	-
A4	-	-	-	-
B1	62.3	2170	0.616	29043
B2	102.5	6.06	1.023	5.43
B3	100.0	6.06	1.020	4.14
B4	102.2	6.01	1.023	5.33
C1	102.3	6.05	1.023	5.96
C2	77.5	6.31	1.020	2.56
C3	102.0	4.90	1.030	2.64
C4	102.7	4.76	1.023	2.49
D1	-	-	-	-
D2	102.0	5.98	1.020	2.55
D3	100.0	4.66	1.003	2.89
D4	102.3	4.22	1.023	2.32

Table 7.2: Details of the different sheet resistances and the supply currents when samples used in the ion-implanted ohmic contact study were tested at room temperature (RT) and 4K. Samples that have blank spaces failed to conduct.

energy of 180 keV and produces samples that work both at low temperature (4K) and at higher temperatures.

The lowest temperature anneal of 750°C only gives low resistance values for R_{sheet} for the wafer with the 8×10^{14} cm^{-2} P implantation at 100 keV. Whilst the sheet resistances from samples with a 900°C anneal would seem to indicate that this high temperature anneal is similar to the 850°C anneal in terms of device performance, it must be noted that samples annealed at 900°C gave very noisy results. The optimum anneal temperature appears to be around 850°C. Whilst the 30 s anneal and the 60 s anneal appear to give quite similar results, the shorter anneal gives slightly better R_{sheet} values. It must be noted that the effect of the anneal on dopant diffusion is not assessed and other more elaborate measurements are required to assess the degree of strain relaxation that occurs.

Based on the results presented in Table 7.2, the recommended empirical dose and implantation energy for P ion-implanted ohmic contacts was 8×10^{14} cm^{-2} dose at either 100 keV or at 180 keV. Ion implantation at 180 keV may cause more damage to the wafer surface but they will have a greater range and a larger penetration depth.

7.4 Sample Designs and Device Fabrication

7.4.1 Sample Designs

The novel technique that is used in producing the selective area implanted devices requires careful consideration of wafers and device geometry. Patterning is a crucial stage, both during the ion implantation of dopant and ohmic contacts and in subsequent sample lithography. This section outlines some of the work and designs used for designing and creating suitable electron beam patterns and compatible lithography masks.

All of the Hall Bar designs used are based upon a standard Hall bar geometry normally used in device assessment. In order to maximize the yield of devices per wafer and to facilitate device handling, devices on chips with dimensions of 2.6 mm × 2.3 mm were produced. Figure 7.5 shows the Hall bar shape, formed by patterning with an electron beam and ion implantation As, together with the ion implanted P regions. The annealed metal deposited on the sample surface forms a physical contact and is also shown. The P ion implanted ohmic contacts should be aligned to the corresponding contact areas on the buried Hall bar. The

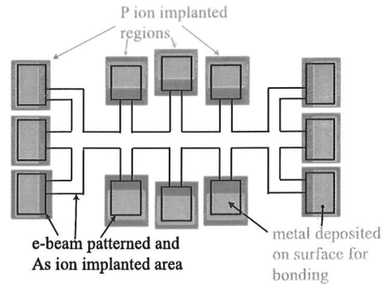

Figure 7.5: The Hall bar shape, formed by patterning with an electron beam and doped with ion implanted As is shown, together with the ion implanted P regions. The annealed metal deposited on the sample surface forms a physical contact and is indicated.

P implanted areas are slightly larger than the contact area on the electron beam defined Hall bar, so that even if precision alignment does not occur, there should still be some overlap.

The electron beam patterns and mask set were designed using LASI, a shareware program[1], that allows the complex design of integrated circuits. LASI was used since it is able to correctly output the GDS-II file types required by the electron beam patterning system. The mask set K7557, which was designed to be used with selective area doped devices, was fabricated commercially by Compugraphics International Limited. The mask fits over the alignment marks and enables accurate deposition of surface contact metal over P ion implanted ohmic contact regions. It also allows the alignment of surface gates.

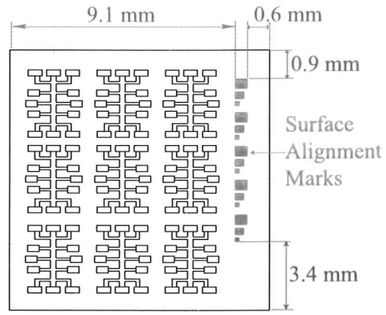

Figure 7.6: A 3 × 3 array of Hall bar devices. Each block of 9 Hall bars has one set of alignment marks.

[1]LASI can found at *http://cmosedu.com*

During the electron beam stage the entire wafer is patterned. In order to simplify device processing the Hall bars are set in 3 × 3 arrays, each with one set of alignment marks for each block of nine devices, as shown in Figure 7.6. The overall block of nine has an area which is 10 × 10 mm^2 for easy handling.

7.4.2 Modified Device Fabrication Process

The device fabrication process is a simplified version of the one outlined in Section 3.3. The first step was to identify and isolate the required block of nine Hall bars, using the surface alignment marks. Ohmic contacts were formed by following the procedure outlined in Section 3.3.3. Approximately 200 nm of Al(1% Si) was deposited on the samples and samples were annealed for 10 minutes at 400°C.

It is slightly easier to form surface gates since the deposited Al(1% Si) ohmic contacts can be used to help alignment. If the gate pattern did not overlap the ohmic contacts, 100 nm to 150 nm of Al(1% Si) was deposited on the wafer surface. The passivating oxide was kept to try and reduce gate leakage to the 2DEG and the surface gates were not annealed. The processed sample was cleaved into separate devices and individual Hall bars were affixed to LCC packages with silver dag and then bonded with Au wires.

7.5 2DEG Magnetotransport Results and Discussion

7.5.1 2DEG Hall Bar

Standard Hall bar devices were fabricated from the selective area ion implanted wafers. All of samples had deposited metal surface contacts that had been annealed at 400°C for 10 minutes. The processed devices were tested in magnetic fields of up to 8 T in order to determine the transport properties.

All of the standard Hall bar samples were found to be conducting down to low temperatures of 1.5 K and illumination with a red LED had little effect on the mobilities and carrier densities. Figure 7.7 shows the best longitudinal (ρ_{xx}) and Hall resistivities (ρ_{xy}) that were obtained from a sample with a 5 nm spacer and As ion implantation dose of 2 × 10^{13} cm^{-2}. The sample shows a Hall mobility of 49 000 cm^{2}V^{-1}s^{-1} for a carrier density of 9.7 × 10^{11} cm^{-2} (electron mean free path = 0.55 μm). Figure 7.8 shows the best longitudinal (ρ_{xx}) and Hall resistivities (ρ_{xy}) that were obtained from a sample with a 12 nm spacer and As ion implantation dose of 4 × 10^{13} cm^{-2}. The sample shows a Hall mobility of

25 000 cm^{2}V^{-1}s^{-1} for a carrier density of 7 × 10^{11} cm^{-2}. These measurements were taken in 8 T perpendicular magnetic field at 1.5 K in the dark. Well defined SdH oscillations in ρ_{xx} and QHE effect plateaux are evident in ρ_{xy}, in both figures. At a slightly higher temperature of 4 K, all of the samples were parallel conducting.

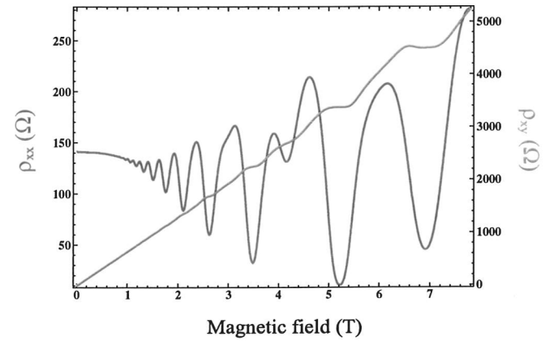

Figure 7.7: Longitudinal and Hall resistivities at 1.7 K for selective area, ion implanted, inverted 2DEG samples. The sample gives a Hall mobility of 49 000 cm^{2}V^{-1}s^{-1} for a carrier density of 9.7 × 10^{11} cm^{-2}. The measurements were taken in 8 T perpendicular magnetic field at 1.5 K in the dark using a sample that has a 5 nm spacer. The sample has been ion implanted using As at 100 keV, with a dose of 2 × 10^{13} cm^{-2}.

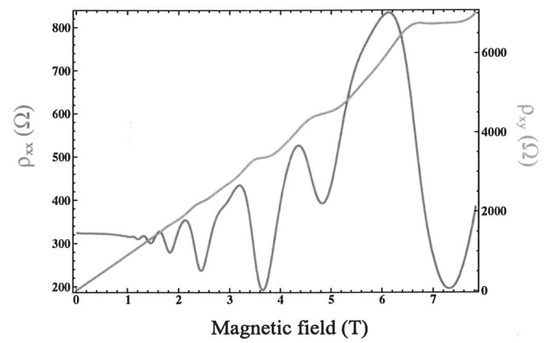

Figure 7.8: Longitudinal and Hall resistivities at 1.7 K for selective area, ion implanted, inverted 2DEG samples. The sample gives a Hall mobility of 25 000 cm^{2}V^{-1}s^{-1} for a carrier density of 7 × 10^{11} cm^{-2}. The measurements were taken in 8 T perpendicular magnetic field at 1.5 K in the dark using a sample that has a 12 nm spacer. The sample has been ion implanted using As at 100 keV, with a dose of 4 × 10^{13} cm^{-2}.

The quantum lifetime, τ_q and α have been calculated for the sample shown in Figure 7.8. These give $\tau_q = 0.9$ ps and $\alpha = 4.5$. This indicates that the scattering mechanisms are still dominated by remote ionised impurity scattering and surface roughness scattering. However the quality of all of the processed samples are inhibited by a regrowth interface. As has been discussed in previous chapters, the regrowth interface has a strong effect on the mobility and carrier density and as the regrowth interface is brought closer to the well it has a detrimental effect on the carrier density and Hall mobility. Since the ion implanted regions is at the regrowth interface, the spacer thickness between this interface and the quantum well is even more significant and is discussed in Section 6.4. As the spacer thickness decreases, the doped region becomes closer to the quantum well and it will be easier to excite carrier into the well, giving a large carrier density. However the increased proximity of the doped region to the well will increase the remote ionised impurity scattering.

The magnetotransport results are consistent with the results presented in chapter six. In order to obtain higher quality samples using this technique, design improvements to the inverted structures need to be made. Chapter six shows that there is a clear relationship between the implantation energy and dose, spacer thickness and the low temperature transport properties . For improved selective area doped sample mobilities, wafers need to be prepared which have been produced using optimum ion implantation doses and energies. These need to be modelled and verified experimentally.

7.5.2 Ohmic Contact Anneals

The wafers that have been fabricated using this technique have a P ion implanted path from the wafer surface to the patterned 2DEG. Deposited Al(1% Si) metal was used to form a surface contact to the P ion implanted region. Implanted P ions form a path to the 2DEG and the surface metal is needed to form a physical contact as shown in Figure 7.9. However, the degree of P/Al/SiGe intermixing required to form good ohmic contacts, is not known. An investigation was carried out into the effect of the anneal temperature and duration on the transport properties and to possibly give an insight into the role of the deposited metal in ohmic contact formation.

Devices have been fabricated where the surface metal was not annealed. These were tested in order to determine whether a non diffused metal/doped semicon-

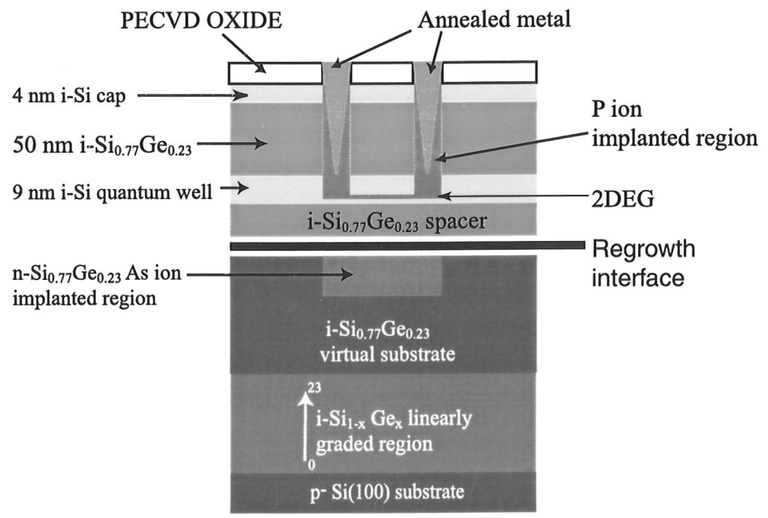

Figure 7.9: A cross section of a completed device. The selectively patterned doped region is shown together with the P ion implanted region. Annealed metal that has been deposited on the wafer surface is used to form physical contacts.

ductor interface alone would form a conducting ohmic contact. It was found that samples without an anneal fail to conduct at any temperature.

It is known that the standard anneal of 400°C for 600 s, used for most samples in this thesis, is sufficient to form working devices. It may be that at this high temperature, annealed metal penetrates down to the 2DEG and that P ions are not necessary. The range and durations used in this investigation were limited to 400°C and 600 s since these are known to form working devices. Higher temperature and increased duration anneals give rise to the possibilities of dopant diffusion as well as strain and lattice relaxation. Certain processing steps such as the resist cure, occur at temperatures around 150°C, so the minimum temperature anneal used in this investigation was 200°C.

Two series of devices were produced simultaneously, that only differed by their anneal temperature or anneal duration. In the first series each device was annealed at 400°C for varying times. Samples in the first series (A1) were from a wafer with a 5 nm spacer and ion implantation dose of 2×10^{13} cm^{-2}. In the second series, each device was annealed for 600 s but with a different anneal temperature. Samples in the second series (A2) were from a wafer with a 12 nm spacer and ion implantation dose of 4×10^{13} cm^{-2}.

Results

Samples from both series of devices were as measured in the dark at 1.5 K in magnetic fields of 8 T and the results are shown in Table 7.3. An examination of the table shows that a low temperature anneal of 200°C gives values that are similar to a 400°C anneal. All of the samples in the first series have fairly similar carrier densities but varying mobilities. There should be no reason for a reduced mobility for anneals between 200°C to 400°C and further investigation needs to be carried out to ascertain whether this is just a statistical variation.

An examination of the second series of devices in table 7.3, shows that all of these devices show a lower carrier density and mobility than the first series. This is consistent with the results presented in chapter six, where it is shown that a larger spacer and increased ion implantation dose have a detrimental effect on the mobilities. Table 7.3 shows that there is a cut off point for anneal duration, below which the samples fail to conduct. Samples with anneals of less than 120 s failed to conduct at all, even with extensive illumination. An increased duration anneal seems to have little further effect on the transport properties. This suggests that only a short temperature anneal, greater than a minimum value, is sufficient to passivate any surface states and allow the necessary metal/semicondutor inter-diffusion required to form an ohmic contact.

Wafer	Anneal Temperature (°C)	Anneal Duration (s)	n_s $\times 10^{11}$ cm^{-2}	μ cm^{2}V^{-1}s^{-1}
A1	200	600	9.72	49 928
A1	250	600	9.62	45 911
A1	300	600	9.5	35 521
A1	350	600	9.8	43 579
A1	400	600	9.65	49 579
A2	400	60	-	-
A2	400	120	7.67	25 061
A2	400	300	7.60	22 809
A2	400	450	7.33	22 421
A2	400	600	7.11	25 114

Table 7.3: The mobility (μ) and carrier density (n_s) as measured in the dark at 1.5 K, for samples with varying anneal temperatures and duration. Blank spaces (-)indicate that the samples did not conduct.

It is difficult to ascertain the exact role played by the P column. There is not as much metal diffusion with a reduced duration anneal or with a low temperature anneal and it is possible that the P ions will compensate for this. Similar tests with control samples that do not contain a P ion ohmic contact implants, show either a lack of conduction or very poor transport properties at 1.5 K.

Within the limits of this analysis, it has been shown that the P ion columns have a significant effect. Samples that have a P ion implanted ohmic contact region and which have been given low duration and low temperature anneals, have been used to form working devices.

A true check to see if the P ion columns have an important role, would be to grow two sets of wafers that have been patterned using selective area ion implantation and to only use P ion implantation for contacts with one wafer. Alternatively, to allow a direct comparison, only part of a wafer would be patterned with P ions. A pattern design could be used that would only ion implant P into some of the contacts on individual devices, leaving other contacts free from implantation. This would allow the direct comparison of P ion implanted and non ion implanted ohmic contacts, that would have been subjected to identical growth and processing conditions. However the selective patterning process is very expensive and it is estimated that the cost of a single wafer produced using this technique is currently in excess of 10,000 pounds[2].

7.6 One Dimensional Channels

One area of significant interest is in one dimensional electron behaviour. This allows the investigation of effects such as ballistic transport, which occurs when scattering by impurities can be neglected and the constriction width and constriction length are smaller than the electron mean free path, l.

1D structures were first lithographically defined in the accumulation layer of an n-channel Si-MOSFET by Fowler [156]. A narrow n-channel was flanked by two heavily doped p^+ regions and the application of a negative voltage with the p^+ regions provided lateral confinement. In order to observe this effect surface Schottky split gates with a narrow gap were fabricated above a 2DEG and low temperature conductance was monitored as a function of gate voltage. With the application of a negative voltage the 2DEG is depleted from beneath the

[2] *Private communication-* Dr. A. C. Churchill, DERA

gates leaving a narrow conducting strip between the gate fingers connected to a 2DEG reservoir. Such a device has been demonstrated in Si/SiGe [157], but the mobility of the material used did not match those now available, resulting in 1D quantisation which was not clear.

As early as 1988, Wharam [87] and Van Wees [88] both discovered that the conductance in short and narrow constrictions are quantised in terms of a universal value of $\frac{2e^2}{h}$ in GaAs ($G = \frac{g_s g_v e^2}{h} N$ and in GaAs $g_s = 2$ and $g_v = 1$). For the case when transport is ballistic, it can be seen that negatively increasing the surface gate voltage causes the conductance, G, to jump in intervals of $\frac{2e^2}{h}$. Eventually the transport channel is fully depleted and the channel pinches off. Many comprehensive reviews on this topic are available (for a list see [62]).

The technique outlined in this chapter can be used to physically define narrow constrictions during the dopant implantation stage of the wafer growth process. These constricted regions on the Hall bar are shown in figure 7.10. Also shown are two photographs that have been taken after the ion implantation stage and oxide strip. The photographs show that high resolution electron beam lithography can be used to define small features.

The normal method for producing 1D constrictions relies on knowing the carrier density and electron mobility of the wafer and this allows the calculation of the electron mean free path. Then it is possible to calculate the correct dimensions needed when fabricating surface split gates for ballistic transport. Since material properties of the fabricated wafer are not known before wafer growth it is difficult

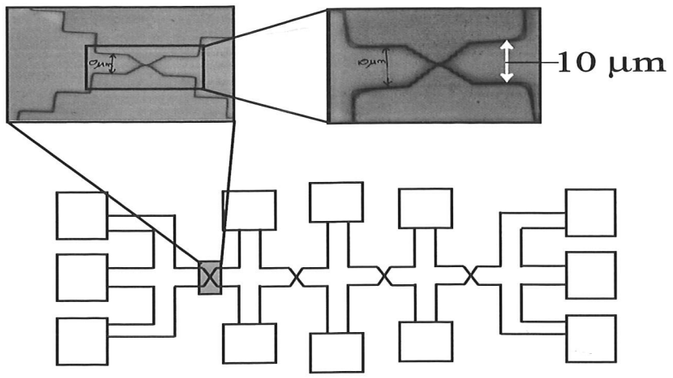

Figure 7.10: Constricted regions on the Hall bar are shown in the schematic as well as two photographs. The photographs have been taken after the ion implantation stage and oxide strip.

to design structures that might show ballistic transport. Modelling programs were used to provide an estimate of the likely carrier density and possible electron mean paths. A lot of samples with differing constriction lengths, CL and widths, CW were fabricated and it was hoped that by having a variation in the constriction dimensions, some of them would have CL and CW smaller than the electron mean free path, l. The minimum resolution is limited by the electron beam resolution and the minimum feature size used was 0.2 μm.

This technique relies heavily on the use of surface gates. When surface split gates are used to form narrow channels, the application of a voltage can be used to electrostatically vary the width of the constriction. However, the surface gates that were used cover the entire Hall bar region and thus cannot be used to vary the channel width. It was hoped that the surface gate can be used to change the carrier density in the device and in this way, vary the number of electrons in the narrow channel.

7.6.1 Results and Discussion

The peak results obtained from 2DEG samples possessing dopant regions that have been selectively patterned in Section 7.5.1, indicate that the wafers used yield a maximum mobility of only around 50 000 $cm^2V^{-1}s^{-1}$ for a carrier density of around 1×10^{12} cm^{-2}. The largest electron mean free paths that can be obtained are between 500 nm to 600 nm. Other wafers have a much lower mobility and hence have a much lower mean free path between 200 nm to 400 nm and this limits the number of devices per wafer that might show quantised conductance.

The smallest feature sizes that were defined using the electron beam had CL = 0.2 μm and CW = 0.2 μm. This gives a severely restricted range of devices that might exhibit 1D ballistic behaviour. Only devices, with constriction lengths and widths of between 200 nm and 600 nm, from a wafer with 5 nm spacer and ion implantation dose of 2×10^{13} cm^{-2} were used.

Most devices failed to conduct at all at room temperatures or at low temperatures. Small feature devices are very sensitive to stray voltages and the application of a small bias such as when probing devices is enough to destroy them. This can be a problem when bonding devices, since stray voltages can sometimes be discharged across a device and are sufficiently strong to destroy the devices. Although a great deal of care and vigilance was exercised in device fabrication, only a small yield of working devices was obtained.

The only samples to conduct at low temperatures were from devices that had CL or CW values of around 500 nm. All devices with construction lengths and widths of less than 500 nm failed to conduct at all. When using the surface split gate technique with electrostatic depletion, the initial wide channel will be populated and as the channel width is reduced, carriers remain in the channel. However this technique assumed that there would be a large enough carrier density in the constricted region for conduction. Effects such as interface depletion mean that the width of the wires may be smaller than anticipated. If very thin constrictions are used the entire channel may be closed and hence the devices will fail to conduct at all, even if a large positive bias is applied. It is probable that the majority of samples which fail to conduct have been destroyed in the processing and bonding stage. It is also assumed that during the wafer patterning and growth and during device processing that the alignment was accurate. If even a small degree of misalignment occurred during wafer growth or device processing then the devices may have CL and CW values that are different to the designed values.

Figure 7.11 shows results from a device that has $CW = 500$ nm and $CL = 300$ nm. The applied voltage is across a surface gate that covers the whole device and covers four constrictions. The plot shows the conductance when measured across constricted regions and across the width of the Hall bar. Figure 7.11 shows that these cannot be readily distinguished from each other. When using ohmic contacts across the width of the Hall bar (across a 2D region) the conductance

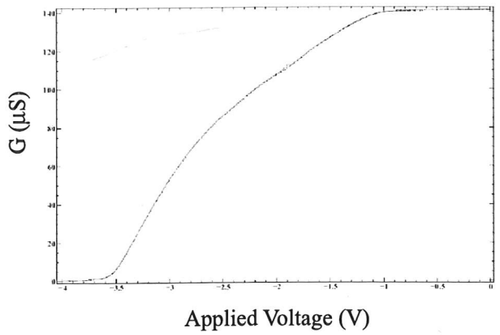

Figure 7.11: Conductance measurements for a sample that has constriction widths of 500 nm and constriction lengths of 300 nm. The measurements at 4 K in the dark using a sample that has a 5 nm spacer. The sample has been ion implanted using As at 100 keV, with a dose of 2×10^{13} cm^{-2}.

trace is the same as that across a constricted region.

The conductance saturates at voltages greater than -1 V and higher voltages do not have any effect. The application of a positive bias has no effect on the conductance. Below -1 V, negative biases across the surface gate have a significant effect on the conductance. As an increasingly negative bias is applied, electrostatic depletion causes a decrease in conductance, G, up to -3.5 V at which point the channel is fully depleted and no conductance is observed. No conductance plateaux can be seen in the plot and 1D ballistic behaviour is not evident in these results.

All samples show very high leakage to the 2DEG, which is probably due to a mistake made in the patterning stage. The surface gate pattern was fabricated on mask K7557 was designed to enhance 2DEG mobilities. As a result it overlaps the P ion implanted region of every ohmic contact and so the surface gate design may be responsible for the high degree of leakage.

It has been shown that with a wide enough constriction there is conductance, but better mobility wafers will be needed to see any 1D ballistic transport. Also more work needs to carried out into finding out the minimum feature sizes that can be produced with this technique. New surface gate designs are needed, that do not overlap the P ion implanted regions. Without some form of surface split gate near the constricted region, the size of the constriction cannot be readily varied. A better surface gate mask needs to be designed and since precision alignment is needed it would have to be made commercially. Any masks made in-house using optical lithography would not be able to give high resolution that is required for accurate alignment.

7.7 Conclusions

The technique of selective area doping using *ex-situ* ion implantation and regrowth has been demonstrated in this chapter. This technique has been successfully used to define Hall bar shapes and to produce 2DEG samples that conduct at low temperatures of 1.5 K. If ion beams with an improved resolution could be used, then this technique could be further improved.

The working 2DEG devices demonstrate Hall mobilities of 50 000 cm^{2}V^{-1}s^{-1} for carrier densities of 1×10^{12} cm^{-2} and show that the selective area patterning technique has been successfully applied. The performance of the fabricated

devices is limited by the design of the wafer structure. Devices with improved electronic properties could be obtained if optimised inverted 2DEG structures were used.

The variation of anneal temperatures and duration in Section 7.5.2 shows that the P ion columns have a significant effect on the electronic properties of the devices. Samples possessing P ion implanted ohmic contact regions can be given low temperature anneals and can still produce working devices which have performances matching devices which have been given the standard anneal. Tests with samples that have been given anneal durations show that if the anneal is too short, then ohmic contacts will not be formed and the sample will fail to conduct. It has been shown that a short duration anneal of around 120 s is sufficiently long enough to form ohmic contacts and that further increasing the anneal duration does not enhance device performances. As long as the short anneal is greater than a minimum value, it is sufficient to passivate any surface states and allow the necessary metal/semicondutor inter-diffusion required to form an ohmic contact. However further investigation is required to ascertain the exact role of the P atoms in the ohmic contact.

The patterning process can be used to define small sub-micron geometries and features, but it has been difficult to produce conducting samples. Many samples have been destroyed during device fabrication. The wafers used in this study are limited by electron mean free paths of around 600 nm and restrict the range of devices that can be used to investigate ballistic transport. The devices that were tested show that samples with a constriction length and width of less than 500 nm fail to conduct at all. If a wide enough constriction is used then samples will conduct. Samples which have a constriction width of 500 nm or more will conduct but there is no evidence of any 1D quantisation of conductance. This is attributed to errors in the surface gate pattern. To see any 1D ballistic transport, improved wafer structures are required together with improved surface gate designs.

It has been shown that it is possible to incorporate a technique that requires precision alignment within a conventional growth process. This technique has been used to define dopant regions in exact areas of a wafer and thus simplify post-wafer growth device fabrication. This chapter has shown how it is possible to dope very small areas on a wafer and that is possible to fabricate working devices from such wafers.

Chapter 8

Conclusions and Further Work

8.1 Conclusions

The work in this thesis focuses on Si/SiGe 2DEG wafers that have been grown in a two stage process. A virtual substrate is grown and then removed from the UHV compatible CVD growth chamber. After a chemical clean, the wafer is returned to the growth chamber for the growth of the Si quantum well and other heterolayers. The successful incorporation of a regrowth interface in a modulation-doped Si/SiGe 2DEG has been demonstrated and the effect of this regrowth interface on device transport properties has been investigated. This work shows that *ex-situ* processing during a growth sequence is possible, which in turn offers greater flexibility in wafer fabrication. Impressive low temperature Hall mobilities of 260 000 $cm^2V^{-1}s^{-1}$ for carrier densities of 3.6×10^{11} cm^{-2}, have been attained in 2DEG samples containing a regrowth interface. This shows that difficulties normally encountered in treating a virtual substrate as a normal substrate, have been overcome.

In order to avoid contamination of the UHV compatible CVD chamber, any wafer that has been processed *ex-situ* needs to be chemically cleaned before it can be returned to the growth system. This cleaning process produces a passivating surface oxide, which must be removed from the wafer surface before growth can recommence. A lower temperature desorption of the passivating chemical oxide has been found to improve the material quality and hence the transport properties.

The incorporation of a regrowth interface has a detrimental effect on the transport properties causing increased surface roughness and more scattering from the

interface itself, which causes a reduction in Hall mobility and carrier density. However, results indicate that the reduction in mobility for thin buffers samples is only 62 % when compared to conventional 2DEGs. The proximity of the interface to the quantum well has a direct effect on the transport properties since the Si enriched interface is believed to contain charged traps. As the buffer thickness between the quantum well and the regrowth interface decreases, it becomes easier for electrons to become trapped at the regrowth interface, leading to a decrease in carrier density and mobility.

Wafers that contain a regrowth interface were used to look into the effect of using a stepped composition substrate and were compared to wafers that have been linearly graded to the bulk Ge content, x, of the $Si/Si_{1-x}Ge_x$ virtual substrate. Results indicate that wafers with matched linearly graded substrates suffer from less strain than wafers that have even a small mismatch. The increased strain caused by the mismatch in Ge content, leads to a decrease in the mobility and the carrier density.

In an ideal wafer there would be no variation in the structure or the material properties across it, as this would increase the yield of high performance. The DERA UHV compatible CVD system used to grow most of the wafers used in this thesis, produces a temperature gradient across the substrate during growth. The importance of growth temperature on wafer structure and material properties was shown in chapter five. This variation in growth temperature of the substrate is found to have a clear effect on the structure of the DERA wafer and hence the transport properties. The higher temperature at the centre leads to thicker layers and a lower Ge content, when compared to the wafer edge. Since the dopant concentration is constant across the wafer, a narrower spacer between the doped region and the quantum well at the edge leads to an increased carrier density in samples taken from that part of the wafer.

Samples with thinner layers have been shown to be affected more by electron scattering mechanisms. The dopant atoms are closer to the quantum well at the wafer edge, and hence samples will be more prone to remote ionised impurity scattering. A narrower quantum well, found at the wafer edge, will suffer from increased interface roughness scattering. The regrowth interface is also much closer to the Si well, which also increases the interface roughness as well as leading to greater surface roughness scattering. This has been used to explain the decreasing mobility at the wafer edge for samples taken from wafers grown by

DERA.

A combined *ex-situ* ion implantation and regrowth technique has been developed. *Ex-situ* doping circumvents the need to introduce dopant into the growth chamber and avoids dopant segregation problems. The feasibility of using *ex-situ* ion implantation as a means of providing a modulation-doped layer, has been shown by the fabrication of inverted n-type $Si/Si_{0.77}Ge_{0.23}$ heterostructures, that conduct at low temperatures of 1.5 K. This technique verifies that virtual substrates can be treated like conventional Si substrates and that it is possible to incorporate *ex-situ* processing within wafer growth and still yield working devices.

The effect of ion implantation of dopant on the transport properties has also been explored. As a general trend, if the ion dose is less than 2×10^{13} cm^{-2}, it is difficult to excite carriers into the quantum well and low temperature conduction only occurs after the electrons have been photo-excited. This could be due to an insufficient amount of carriers transferred from the modulation-doped layer or the presence of charged traps created either by ion implantation damage or at the growth interrupt where *ex-situ* cleaning has occurred.

The spacer thickness between the doped region/regrowth interface and the strained Si well was shown to be very important. If the spacer thickness is too large then the carrier density in the quantum well is too low for device conduction. Even if a very thin spacer is used, it still may not be possible to produce working devices, if the ion implantation dose and energy are low. If a sufficiently high ion implantation energy and dose are used with a thin enough spacer, then working devices can be fabricated. It has been shown that as the spacer thickness is reduced and the regrowth interface approaches the well, charged traps present at the interface lead to a reduction in carrier density.

For a given spacer thickness, as the ion dose increases, so does the sheet carrier density in the strained Si well. However, as the carrier density increases, the mobility falls. The mean-free path is observed to decrease with increasing ion dose, irrespective of spacer layer thickness. This decrease in mobility and electron mean free path is due to increasing remote ionised impurity scattering and interface roughness scattering.

The technique of selective area doping using *ex-situ* ion implantation and regrowth has been successfully used to define Hall bar shapes and to produce 2DEG samples that conduct at low temperatures of 1.5 K. Low temperature Hall mobilities of 50 000 cm^{2}V^{-1}s^{-1} for carrier densities of 1×10^{12} cm^{-2}, demonstrate

in principle that the selective area patterning technique has been successfully applied. The performance of the fabricated devices is limited by the design of the wafer structure and the limitation of the *ex-situ* ion implantation and regrowth process. Improved Hall mobilities and lower carrier densities could be obtained if optimised inverted 2DEG structures were used.

It has been shown that P ion implanted ohmic contacts have a significant effect on the electronic properties of the devices. Samples possessing P ion implanted ohmic contact regions require a very short anneal, sufficient to passivate any surface states. Devices which incorporate P ion implanted contacts, have performances that match devices which have been given a standard anneal. Increasing the anneal temperature or duration in these devices does not enhance device performances.

The patterning process can be used to define small sub-micron geometries and features. Samples which have a Hall bar geometry that possess small constricted regions have been formed. It has been shown that it is possible to produce conducting devices which have constrictions widths that are as small as *500 nm*. Therefore it is now possible to incorporate a technique that requires precision alignment within a conventional growth process. This technique has been used to define dopant regions in exact areas of a wafer and thus simplify post-wafer growth device fabrication. Finally selective area patterning within very small areas has been demonstrated and this can be applied to many areas of research.

8.2 Further Work

The work described in this thesis constitutes a fairly brief overview Si/SiGe heterostructures that contain a regrowth interface. It is clear from the number of questions raised that much work remains to be done in this area. In addition to the points mentioned above, there is scope for extensive study in the many areas outlined below.

Initial investigations into the effects of incorporating a regrowth interface show that the interface may contain charged traps and that the interface itself may lead to an increase in surface roughness. Throughout this thesis a standard chemical clean (the B/CLEAN/R2 described in Section 4.4). It may be possible to improve the surface of the regrowth interface and minimize some of its adverse effects, by modifying the chemical cleaning process. It was shown that a slightly lower temperature oxide desorb is more may be more efficient at removing any residual oxide and improves device performance. The exact relationship between the oxide desorb temperature and the regrowth interface is not known at present and further research needs to be carried out in this area. Ideally a series of identical wafer would be grown and each desorbed with varying temperatures and pressures in order to investigate the effect of the oxide desorb on subsequent electronic properties.

The high Hall mobility obtained with sample 7B22 suggests that higher low-temperature mobilities are possible for appropriately designed and grown samples in the present CVD system. Chapter five shows that thicker layer samples with reduced Ge content, give improved Hall mobilities. Further investigations are required to ascertain whether it is more beneficial to reduce the Ge content or to increase the layer thickness. Modelling results for the DERA 7B22 structure, obtained using TMA-Medici and Silvaco Supreme3 software, are shown in Figure 8.1. This figure shows that lower Ge fractions will provide a carrier density in the quantum well that is sufficiently large enough for conduction. Decreasing the Ge content will reduce the surface roughness and should help to improve the Hall mobility.

All of the wafers used in this thesis incorporate a single regrowth step. Regrowth offers flexible fabrication and could be used to form intricate structures with multiple growth steps, some separated by *ex-situ* chemical cleans. One suggestion for future work would be to grow wafer structures that have two or more regrowth interfaces. If multiple regrowth steps could be incorporated in a single

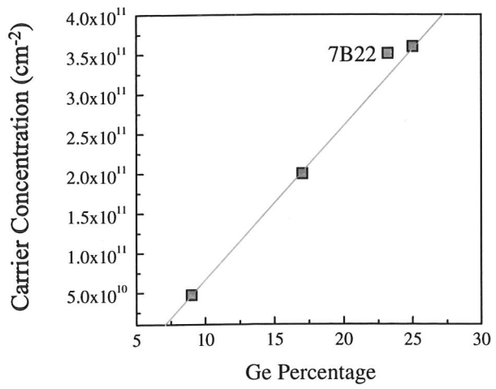

Figure 8.1: Simulation results showing the expected carrier density as a function of the Ge content (and hence the conduction band offset) for the 7B22 Si/SiGe 2DEG structure. This figure was obtained with TMA-Medici software and ion implant models of Silvaco Supreme3 software. Also plotted is the experimental carrier density obtained using samples from 7B22.

structure, it could be used to form devices that have multiple quantum wells.

A technique has been developed that involves the use of *ex-situ* ion implantation in forming a modulation-doped region. This circumvents the need to introduce a dopant species into the growth system and has been successfully used to produce working inverted Si/SiGe 2DEG devices. The highest mobilities attained with the inverted 2DEG samples at 1.5 K, are 73 000 $cm^2V^{-1}s^{-1}$ for a carrier concentration of 4.25×10^{11} cm^{-2}. Clearly there is room for improvement with the blanket ion implanted devices. All of the wafers used in this study have similar structure, with only differing spacer thicknesses between the regrowth interface/ion implanted region and the quantum well. Further investigation into varying other parameters such as the Ge content and growth temperature, might yield devices with improved performances. The importance of the spacer thickness has been emphasised in chapter six and the precise relationship between the spacer thickness and the transport properties is not currently known. One area of further research is to calculate and verify the optimum spacer thickness in inverted 2DEG structures, and in this way improve the transport properties.

In this thesis, it has been shown it is possible to ion implantation of dopant into a SiGe virtual substrate. By varying the energy and dose of the implanted ions, it is possible to control the properties of subsequently deposited layers. In this thesis, modelling was used to try and estimate the optimum ion implantation

energies and doses. Consequently, only a limited range of implantation energies and doses have actually been used. While the results in chapter six have been used to try and identify the exact role of the ion implantation, it would be very useful if further investigations into the effects of the ion dose and implantation energy on the electronic properties. This might also allow make it possible to identify the nature of that electron scattering that occurs and to find out which is the dominant scattering mechanism.

It might also be useful to grow thermally doped inverted 2DEG structures, using the *ex-situ* chemical cleaning process. This would give an insight into whether the regrowth and *ex-situ* cleaning process affects the dopant segregation. A comparison with ion implanted structures would give an insight into the effects of ion implantation on wafer structure and how much damage is caused by the implantation process. It might also give an insight into whether the implantation and subsequent annealing process, is detrimental to the structure and the material properties.

The *ex-situ* ion implantation and regrowth process has been used together with electron beam patterning to form a selective area doping technique. Patterning of the dopant is technique that potentially allows the fabrication of many exotic devices. The main limits to the current technique are the resolution of the electron beam that is currently used for patterning and the ion implantation energies and doses that can be used. Further investigations are required into the minimum feature sizes that can be correctly defined using the current technique.

The selective doping technique outlined in this thesis is still in its early stages and so there is plenty of scope for improvements. At present the technique that is used is a whole wafer process. An additional advantage of using a whole wafer process, is that it is easier to see whether it can be readily incorporated into a commercial system. However a whole wafer process requires a great deal of time and is expensive. If a process could be developed that does not require whole wafers, it would be both cheaper and quicker to use and more convenient for research purposes. A quicker process would speed up the turn-around time between device assessment and implementation of suggested changes in subsequent wafers.

As mentioned above, one area of further study is multilayer systems, in which two or more 2D layers are formed in close proximity. A range of phenomena may be studied in such systems by varying the separation of the quantum wells, and

thereby changing the degree of coupling between the layers. To make best use of such systems requires the ability to make independent contacts to the different layers [158]. The selective doping process together with ion implanted ohmic contacts could be used to form independent contacts to separate layers and this facilitate the production of multilayer systems. The successful demonstration of the use of ion implanted ohmic contacts in chapter seven would suggest that this would be feasible. The working 2DEG results given in Section 7.5.1, demonstrate that the P ions have a significant effect on the ohmic contact. However further investigation is required to ascertain the exact role of the P atoms in the ion implanted ohmic contact. As suggested in Section 7.5.2, a pattern process could be used that would only ion implant P into some of the contacts on individual devices, leaving other contacts free from implantation. This would allow the direct comparison of P ion implanted and non ion implanted ohmic contacts on the same device.

The possibility of incorporating a technique that allows the precise definition of dopant regions on very small areas of a wafer, within a conventional growth process has been demonstrated in this thesis. One dimensional devices are fruitful area for study and the current technique only needs a little improvement to see ballistic or diffusive transport through a narrowed constriction. The wafers that were used to fabricate devices have mobilities of to 50 000 $cm^2V^{-1}s^{-1}$ for high carrier densities of 1×10^{12} cm^{-2} and hence have a poor electron mean free path of only around 600 nm. This severely limited the size of constriction geometries that could be used to try and see 1D quantisation of conductance. The selective area doping technique can been used to define areas as small as 200 nm in exact areas of a wafer, which permits the fabrication of devices that contain small constricted regions. It was found that conduction is possible in samples which have a constriction width of 500 nm, but there is no evidence of any 1D quantisation of conductance. This is attributed to errors in the surface gate pattern that was used, 1D ballistic behaviour might be possible with better quality wafers together improved surface gate and dopant patterns.

In summary, Si/SiGe heterostructures that contain a regrowth interface, have been found to be rich area of study, and there are many possibilities for extending the investigations presented in this thesis.

Appendix A

Ion Implantation Theory

In this section a brief examination of the theoretical ion-solid interaction mechanisms and models are presented. Knowledge of the processes by which energy is transferred from an energetic ion to a solid is fundamental in the understanding of how ion bombardment interacts with a growing film. Issues that are covered in this section include ion stopping mechanisms, ion penetration depths and radiation damage.

Ex-situ ion beam lithography in semiconductors can be achieved by one of two methods. The first is ion implantation induced damage, which is used to define isolated regions within an otherwise conducting device structure. In this case, the energy transferred from the incident ion to the crystal is sufficient to induce electron or hole traps and defects within the lattice.

Alternatively, a dopant species can be implanted into an undoped crystal to define the conducting regions within a device. Often, a high temperature anneal is then required to electrically activate the dopant centres and to remove any damage in the lattice. It is this technique that will be used in the producing of inverted Si/SiGe 2DEG wafers.

A.1 Ion-Solid Interactions

When an ion penetrates a solid it will undergo a series of elastic and inelastic collisions with the atoms and electrons in the target material. Energy lost from electronic (inelastic) collisions produces electronic excitations within the solid. Nuclear (elastic) collisions will result in the displacement of target atoms from their lattice site. These displaced atoms can then produce additional collisions

within the solid (collision cascade) that can result in the sputtering or desorption of atoms from the surface of the target.

The energy of the bombarding ion is an important parameter, since some processes such as defect production have a threshold below which these processes do not occur. A thorough review of this field can be found in '*Ion-solid Interactions: Fundamentals and Applications*' by M. Nastasi, J. W. Mayer and J. K. Hirvonen [159].

A.2 Ion Stopping Mechanisms

The impact of an energetic ion with a solid produces a series of collisions in the target material. In these collisions, the incident particle loses energy at a rate of dE/dX which is determined by screened Coulomb interactions with the target atoms and electrons. Two major mechanisms of energy loss can be distinguished: (i) nuclear collisions, in which energy is transmitted as translatory motion to a target atom, and (ii) electronic collisions, in which the moving particle excites or ejects atomic electrons. The energy-loss rate dE/dX can be expressed as:

$$\frac{dE}{dX} = \left.\frac{dE}{dX}\right|_n + \left.\frac{dE}{dX}\right|_e \tag{A.1}$$

where the subscripts n and e denote nuclear and electronic collisions, respectively. It is customary to refer to a stopping cross-section $S(E)$, which can be thought of as the energy-loss rate per scattering centre. $S(E)$ is defined as:

$$S(E) = \frac{dE}{dX}\frac{1}{N} \tag{A.2}$$

where N is the atomic density of the target material.

Expressions for the nuclear and electronic stopping cross-sections have been proposed by Lindhard [160, 161]. In order to simplify the calculations of the screened Coulomb potentials, Lindhard introduced the concept of a universal reduced cross-section. The nuclear stopping cross-section (in units 10^{-14} eVcm^{2}atom^{-1}) is given by:

$$S_n(E) = 4\pi a_{TF} Z_1 Z_2 e^2 \left(\frac{M_1}{M_1 + M_2}\right) S_n(\varepsilon) \tag{A.3}$$

where a_{TF} is the Thomas-Fermi screening length, Z_1 and M_1 are the atomic number and mass of the incident ion, Z_2 and M_2 are the atomic number and

mass of the recoiling target, e is the electronic charge, and $S_n(\varepsilon)$ is the reduced nuclear stopping cross-section.

The parameter ε is referred to as the reduced energy and is a dimensionless energy unit as given by:

$$\varepsilon = \left(\frac{M_2}{M_1 + M_2}\right)\frac{a_{TF}}{Z_1 Z_2 e^2} E \tag{A.4}$$

where E is the energy of the incident ion (eV).

Physically, ε gives a measure of how energetic a collision is and how close the ion gets to the nucleus of the target atom. $S_n(\varepsilon)$ and a_{TF} are both a function of the screened Coulomb potential between the ion and target nucleus, which is described by the Thomas-Fermi (TF) screening function. Lindhard proposed an approximate analytical solution for the TF screening function and a modification to the screening length to account for the two-atom potential.

While this is a reasonable approximation for calculating stopping powers and cross-sections, a higher level of accuracy over a wider range of reduced energy is obtained from using the Zieger, Biersack, and Littmark [162] (ZBL) universal screening function. The analytical fit to the ZBL reduced nuclear stopping cross-section and the corresponding universal screening length, a_u, are given by:

$$S_n(\varepsilon) = \frac{0.5\ln(1 + 1.1383\varepsilon)}{\varepsilon + 0.01321\varepsilon^{0.21226} + 0.19593\varepsilon^{0.5}} \tag{A.5}$$

$$a_u = \frac{0.8854 a_o}{Z_1^{0.23} + Z_2^{0.23}} \tag{A.6}$$

in which a_u replaces a_{TF}, and a_o is the Bohr radius of the hydrogen atom.

An analytical expression for the electronic stopping cross-section was developed by Lindhard-Scharff (see [163]), and is expressed in reduced notation as:

$$S_e(\varepsilon) = k\sqrt{\varepsilon} \tag{A.7}$$

$$k = \frac{Z_1^{\frac{2}{3}} Z_2^{\frac{1}{2}} (M_1 + M_2)^{\frac{3}{2}}}{12.6(Z_1^{\frac{2}{3}} + Z_2^{\frac{2}{3}})^{\frac{3}{4}} M_1^{\frac{3}{2}} M_2^{\frac{1}{2}}} \tag{A.8}$$

The electronic stopping cross-section can then be obtained by substituting the result of $S_e(\varepsilon)$ into equation A.3, with the Thomas-Fermi screening length being replaced by the Lindhard screening length:

$$a_l = \frac{0.8853 a_o}{\sqrt{Z_1^{\frac{2}{3}} + Z_2^{\frac{2}{3}}}} \tag{A.9}$$

Electronic energy losses dominate at MeV energies, while nuclear processes dominate in the keV range. The above Lindhard models of the stopping cross-sections are based upon a two-body collision process, which assumes violent collisions between atoms of reasonably high energy. Consequently, at lower energies collective effects become increasingly important and the binary collision assumption breaks down. The problems of this many-body collision system can be overcome by molecular-dynamic simulations, however for a first approximation the binary collision model gives a reasonable estimate.

A.3 Ion Ranges

The stopping of an ion in a solid medium is a stochastic process and the collision sequence and subsequent ion deflection varies from ion to ion. As a result, a statistical distribution of the depths to which the ions penetrate is observed.

The actual integrated distance travelled by an ion incident on a semiconductor is called the path length or range, R. The net penetration of the ion into the material is described by a projected range R_p. The difference between R and R_p is illustrated in Figure A.1.

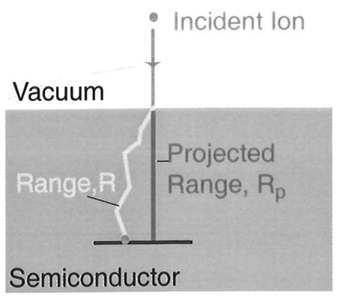

Figure A.1: A schematic drawing for the definition of the projected range, R_p and the path length, R.

A.3.1 Path Length or Range, R

Simple estimates of the average ion range can be obtained by assuming only nuclear stopping process dominate. Neglecting the contributions from electronic stopping the average ion range is described by:

$$R = \int_{E_o}^{o} \frac{dE}{N S_n(E)} \tag{A.10}$$

The ZBL scattering formula for the nuclear stopping cross-sections in reduced notation can be expressed in a power-law form. The associated power law fitting parameters give a more accurate analytical fit to the universal screening potential for different ranges of ion energy. The range is now given as:

$$R = \frac{(1-m)\varepsilon^{2m}}{m\lambda_m} \frac{(M_1+M_2)^2}{4\pi N a_u^2 M_1 M_2} \tag{A.11}$$

where m and λ are power-law variables, ε is the reduced energy, N is the target atomic density, and a_u is the screening length.

It is also possible to express Equation A.10 in terms of the dimensionless units ε and ρ_l

$$\rho(\varepsilon)_l = \int_o^{\varepsilon} \frac{d\varepsilon}{S(\varepsilon)} \tag{A.12}$$

$S(\varepsilon)$ is the reduced stopping range [160] and is given by

$$S(\varepsilon) = S_n(\varepsilon) + S_e(\varepsilon) = S_n(\varepsilon) + \sqrt{k(\varepsilon)} \tag{A.13}$$

The reduced range ρ_l is related to the range, R, by

$$\rho(\varepsilon)_l = RNM_2 4\pi N a_{TF}^2 \frac{M_1}{(M_1+M_2)^2} \tag{A.14}$$

The advantage of using Equation A.12 is that it can be used to establish a universal set of reduced range curves that only depend on ε and the electronic stopping parameter k. The empirical relationship between ε, ρ and k can be found in [164]. Table A.1 gives the ρ values as a function of ε and k. Table A.2 shows the relationship between the ion implant energy E (in keV) and ε and k for B, P and As ions into a Si or a Ge substrate. Once ε and k have been calculated, ρ (which can be found using table A.1) can be used to determine the range of energetic ions into either Si or Ge.

ε	$k = 0.0$	$k = 0.1$	$k = 0.12$	$k = 0.14$	$k = 0.2$	$k = 0.3$	$k = 0.4$	$k = 1$
0.01	0.072	0.069	0.069	0.068	0.067	0.064	0.602	0.052
0.02	0.115	0.110	0.109	0.108	0.106	0.102	0.098	0.081
0.05	0.218	0.207	0.205	0.203	0.197	0.188	0.108	0.144
0.10	0.360	0.339	0.335	0.332	0.321	0.304	0.289	0.224
0.20	0.614	0.571	0.563	0.553	0.533	0.501	0.472	0.353
0.50	1.35	1.21	1.19	1.17	1.10	1.01	0.938	0.656
1.0	2.67	2.29	2.22	2.17	2.01	1.80	1.63	1.06
2.0	5.84	4.57	4.39	4.22	3.79	3.26	2.88	1.71
2.0	19.4	11.9	11.1	10.4	8.83	7.11	5.99	3.17
10.0	53.6	23.8	21.6	19.9	16.1	12.3	10.1	4.92

Table A.1: The value of ρ as a function of ε, and k for B, P and As into Si and Ge

ion	ε/E (keV) Si	ε/E (keV) Ge	ρ/R (μm) Si	ρ/R (μm) Ge	k Si	k Ge
B	0.113	0.049	32.2	10.6	0.22	0.47
P	0.021	0.012	29.0	15.7	0.14	0.024
As	0.0048	0.0034	17.0	14.8	0.12	0.16

Table A.2: ε, ρ and k for B, P and As ions into Si and Ge substrates

A.3.2 Projected Range, R_p

In many applications the projected range, R_p, is the quantity of interest. The projected range is defined as the total path length of the projectile measured along the direction of incidence. An approximate measure of the stopping range can be found using the theory of Lindhard *et al.* [160], which gives

$$R_p \cong \frac{R}{(1 + \frac{M_2}{3M_1})} \tag{A.15}$$

Projected range corrections for B, P and As ions into Si and Ge substrates are summarised in Table A.3

A.3.3 Range Straggling, ΔR_p

Ion implantation is a random process and the mean projected range, R_p is the most probable location for an ion to come to rest. The uncertainty in the scattering process as the ion travels through the target gives rise to ions coming to

Ion M_1	Substrate M_2	R_p/R 20 keV	R_p/R 40 keV	R_p/R 100 keV	R_p/R 500 keV	Rule of thumb value $(1 + M_2/3M_1)^{-1}$
B	Si	0.57	0.64	0.73	0.86	0.54
P	Si	0.72	0.75	0.79	0.86	0.77
As	Si	0.83	0.84	0.86	0.89	0.89
B	Ge	0.34	0.40	0.50	0.71	0.30
P	Ge	0.50	0.52	0.58	0.71	0.56
As	Ge	0.67	0.69	0.72	0.77	0.76

Table A.3: Projected range corrections, R_p/R, for B, P and As ions into Si and Ge substrates

rest at distances less than and greater than R_p. The average fluctuations in R_p is called range straggling, ΔR_p. Using the theory of Lindhard *et al.* [160], an estimate for ΔR_p can be found using;

$$2.5\Delta R_p \cong 1.1 R_p \left[\frac{2\sqrt{M_1 M_2}}{M_1 + M_2}\right] \tag{A.16}$$

A.3.4 Polyatomic Targets

When calculating ion ranges in compound targets, the atomic number of the constituent species is very important. If the atomic species are sufficiently close in atomic number, then the mean atomic number and mass can be substituted into the above equations and can be treated as a monatomic target. If the atomic numbers are appreciably different then a reasonable estimate of the range can be obtained using;

$$R_p(A_x B_y) = N_{alloy}\left[\frac{\frac{R_p(A)}{N_1 A}\frac{R_p(B)}{N_B}}{\frac{yR_p(A)}{N_A} + \frac{xR_p(B)}{N_B}}\right] \tag{A.17}$$

where $x + y = 1$, and $R_p(A)$, $R_p(B)$, N_A and N_B are projected ranges and the atomic densities in pure substrates A and B, respectively and N_{alloy} is the atomic density of the alloy.

A.3.5 Channeling

The above equations concerning the ranges of ions and radiation damage of material is based on the assumption that the stopping medium is amorphous (disor-

dered) and the main parameters when determining the range of ion are its energy, E, the atomic number of the ion, Z_1 as well as the atomic number of the substrate, Z_2. In practice poly-crystalline and mono-crystalline substrates are used and the vibrational amplitude (temperature dependant) of the lattice atoms are also important parameters.

With single crystal substrates like Si and Ge, the orientation of the ion beam with respect to the crystallographic axes of the substrate has a pronounced effect on the range of any incident ion since implantation along a crystal axis can lead to a fraction of the ions penetrating several R_p. Figure A.2 shows the range distribution in Si for 100 keV As implanted with the beam aligned parallel to the <100> crystal axis as the distribution for incident ions away from any channeling direction. The crystal orientation influence on ion penetration is called *channeling* or the channeling effect.

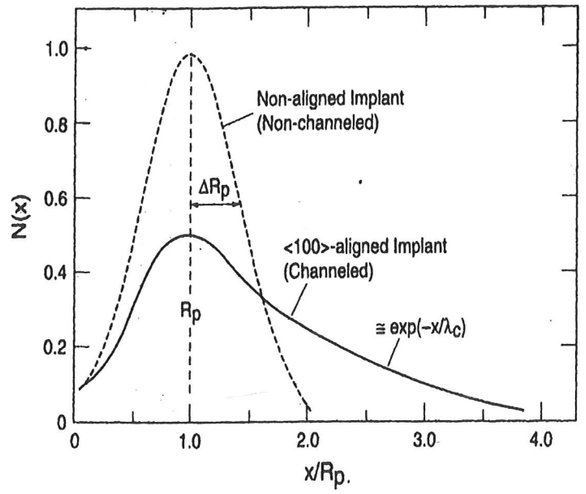

Figure A.2: Range distributions for channeled ions implanted along the <100> axis of Si.The dashed line shows the distribution for incident ions away from any channeling direction.

When an ion is aligned along atomic rows it will travel within the open space, or channels, between the atomic rows. The channeled ions do not make close impact collisions with the lattice atoms and have a much lower rate of energy loss dE/dX and hence a greater range than non-channeled ions.

The channeling distribution depends on surface penetration, substrate temperature, beam alignment and the disorder introduced during the implantation

process itself. It is difficult to avoid channeling effects completely unless the implanted region has been made amorphous by a previous implantation. For a comprehensive review of channeling see [159, 165] and '*Channeling Effects in Ion Implantation*' by R. Simonton and A. F. Tasch in [166].

A.4 Radiation Damage

It has been known for many years that bombardment with energetic heavy ions produces lattice disorder and the disorder can be directly observed by techniques sensitive to lattice structure such as TEM.

As an ion slows down and comes to rest in a crystal, it makes a number of collisions with the lattice atoms and during the course of these collisions sufficient energy may be transferred from the ion to displace an atom from its lattice site. Lattice atoms which are displaced by incident ions are known as primary knock-on atoms and these in turn can displace other atoms creating a cascade of atomic collisions.

This leads to a distribution of vacancies, interstitial atoms and other types of lattice disorder in the region around the ion track. As the number of incident ions on the crystal increases, individual disordered regions begin to overlap and at some point a heavily damaged layer is formed. The total amount of disorder and the distribution depth depends on the ion species, temperature, energy, total dose and channeling effects.

Direction calculations of damage energies in polyatomic atomic materials were first approached by Lindhard [167] who used an approximate method using the mean Z and M values of the substrate atoms. This is a reasonable approximation as long as the differences between Z and M in the target atoms is small. For direct calculations of damage energies in polyatomic materials where there are large differences in the masses of the constituent atoms see [168, 169, 170, 171].

Irradiation damage may be evident in several forms such as point defects (generated by atomic displacement processes during implantation), anti-site defects (where an A atom occupies a site in the B sublattice or where a B atom occupies a site in the B lattice) and dislocations. Line defects, such as dislocation loops have been observed to form in irradiated material due to both defect coalescence and cascade collapse (see '*Theory of Microstructural Evolution* by R. Bullough and M. H. Wood in [172]).

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